

TJA1445

High-speed CAN transceiver with partial networking

Rev. 0.5 — 30 November 2023

Objective data sheet
CONFIDENTIAL

1 General description

The TJA1445 is a high-speed CAN transceiver that provides an interface between a controller area network (CAN) or CAN FD (flexible data rate) protocol controller and the physical two-wire CAN bus. TJA1445 transceivers implement the CAN physical layer as defined in ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5, making them fully interoperable with high-speed classical CAN and CAN FD transceivers. The TJA1445 was developed in compliance with ISO26262, achieving ASIL-B.

The TJA1445 features very low power consumption in Standby and Sleep modes. It supports CAN partial networking by means of selective wake-up functionality as specified in ISO11898-2:2016, making the TJA1445 the ideal choice for CAN system implementations where only nodes that are needed can be activated at any time. Nodes that are not needed for the function being performed can be powered down to minimize system power consumption, even when CAN bus traffic is running.

The TJA1445 includes an SPI for configuration, mode control and diagnostics. The TJA1445B additionally features three general-purpose I/O pins (GPIO) and a CAN transmitter enable/disable input.

The TJA1445 can be configured to ignore CAN FD frames while waiting for a valid wake-up frame. This additional feature of partial networking, called CAN FD passive, is the perfect fit for networks that support classical CAN or CAN FD communications. It allows classical CAN controllers that do not need to communicate CAN FD messages to remain in partial networking Sleep/Standby mode during CAN FD communication without generating bus errors.

2 Features and benefits

2.1 General

- ISO 11898-2:2016, SAE J2284-1 to SAE J2284-5 and SAE J1939-14 compliant
- ISO 26262, ASIL-B compliant
- Partial networking capability through selective wake-up functionality
- Configurable general-purpose I/O (GPIO) pins (TJA1445B)
- Second RXD and/or TXD pins (RXD2/TXD2), configurable via GPIO (TJA1445B)
- Direct transmitter on/off control input (TXEN_N) (TJA1445B)
- Autonomous bus biasing
- Low electromagnetic emission (EME) and high electromagnetic immunity (EMI)
- Qualified according to AEC-Q100 Grade 1
- VIO input for interfacing with 1.8 V, 3.3 V to 5 V microcontrollers
- Listen-only mode for node diagnosis and failure containment
- TJA1445A available in an SO14 package and leadless HVSON14 package with automatic optical inspection (AOI) capabilities
- TJA1445B available in a DHVQFN18 package with automatic optical inspection (AOI) capabilities
- Dark green product (halogen free and restriction of hazardous substances (RoHS) compliant)
- Selectable interrupts on RXD; option to signal only wake-up and power-on related interrupts or all interrupts



- 4-byte general-purpose memory
- SPI system reset
- End-of-line microcontroller flashing support through CAN pins
- Selectable WAKE pin filter time

2.2 Predictable and fail-safe behavior

- Undervoltage detection on all supply pins with defined behavior below the undervoltage thresholds
- Full functionality guaranteed from the undervoltage detection thresholds up to the maximum limiting voltage values
- Transceiver disengages from the bus (high-ohmic) when the battery voltage drops below the Off mode threshold
- Internal biasing of TXD to enable defined fail-safe behavior

2.3 Low-power management

- Very low-current Standby and Sleep modes, with host, local and remote wake-up capability
- Local wake-up via the WAKE pin
- Remote wake-up via a wake-up pattern (WUP) or wake-up frame (WUF)
- Configurable CAN wake-up pattern (dom-rec-dom according ISO11898-2:2016 or dom-rec-dom-rec according to upcoming ISO11898-2:2023 update)
- Wake-up frame according to ISO 11898-2:2016
- Entire node containing the TJA1445 can be powered down via INH while still supporting local and remote wake-up
- Only V_{BAT} is needed to support local and remote wake-up

2.4 Diagnosis and Protection

- Overtemperature diagnosis and protection
- Transmit data (TXD) dominant time-out diagnosis
- Bus dominant failure diagnosis
- Cold start diagnosis (first battery connection)
- High ESD handling capability on the bus pins (8 kV IEC and 8 kV HBM)
- Bus pins and VBAT protected against automotive transients

3 Ordering information

Table 1. Ordering information

| Type number | Package | | |
|-------------|----------|--|-----------|
| | Name | Description | Version |
| TJA1445AT | SO14 | plastic small outline package; 14 leads; body width 3.9 mm | SOT108-1 |
| TJA1445ATK | HVSON14 | plastic thermal enhanced very thin small outline package; no leads; 14 terminals; body 3 × 4.5 × 0.85 mm | SOT1086-2 |
| TJA1445BHG | DHVQFN18 | plastic thermal enhanced very thin small outline package; no leads; 18 terminals; body 3 × 4.5 × 0.85 mm | SOT2163-1 |

4 Block diagram

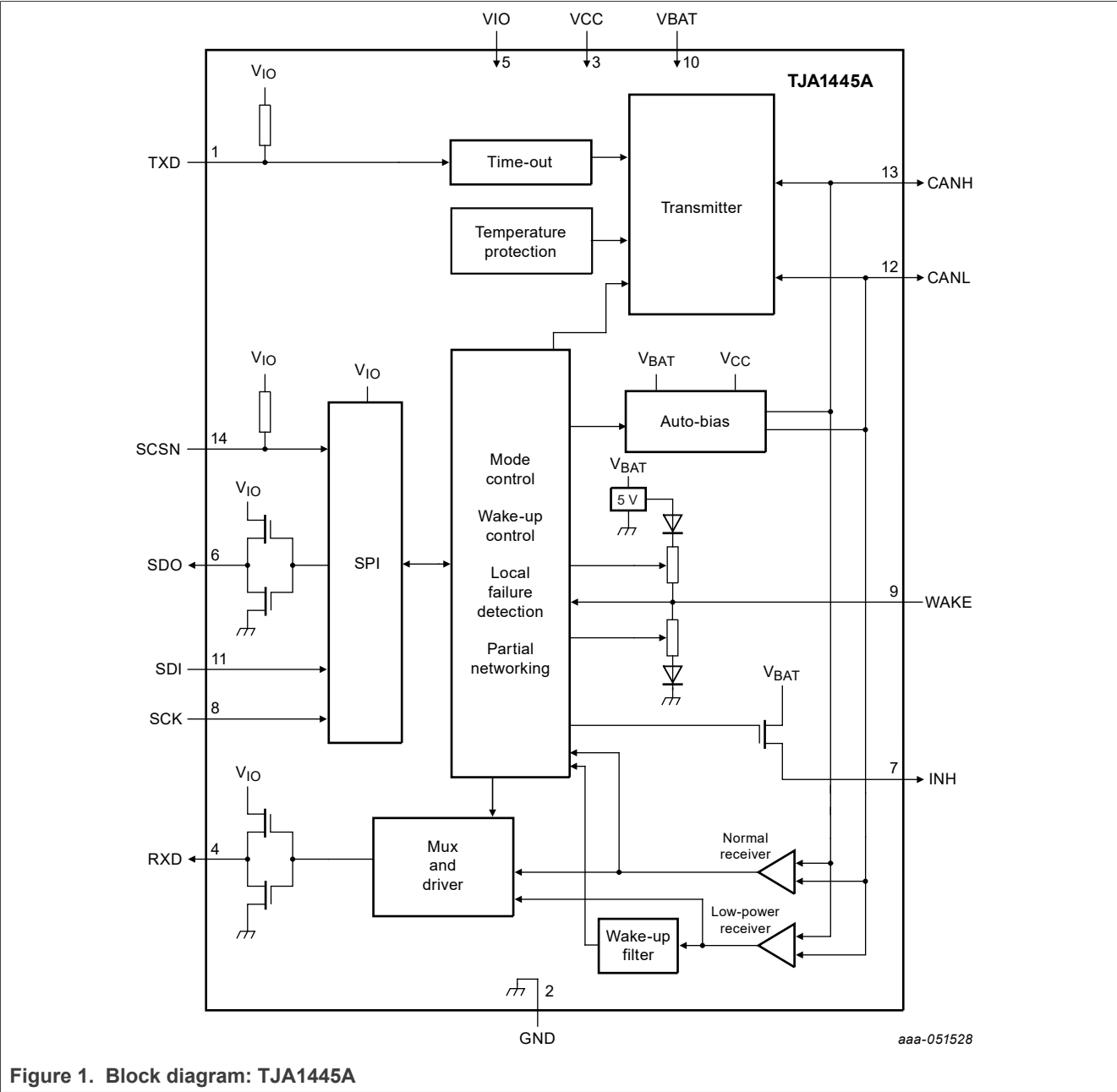


Figure 1. Block diagram: TJA1445A

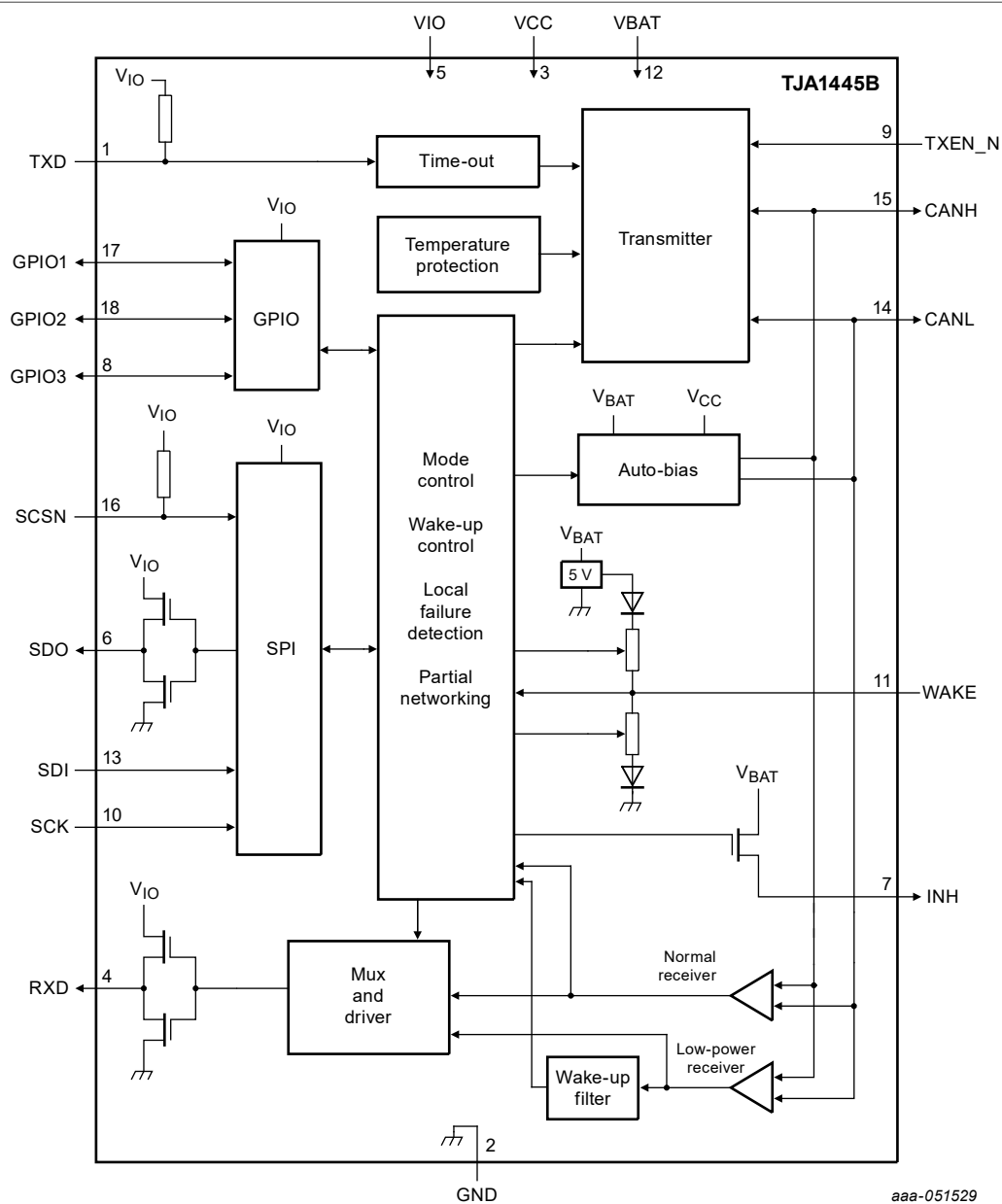
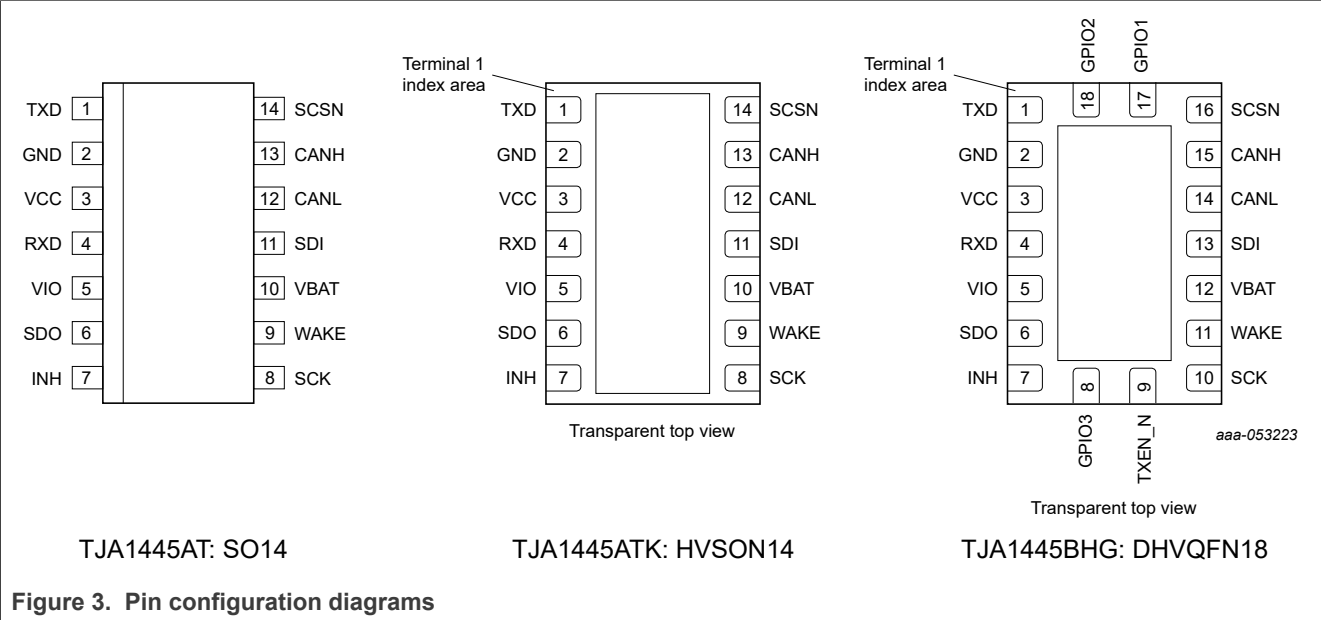


Figure 2. Block diagram: TJA1445B

5 Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description: TJA1445A

| Symbol | Pin | Type ^[1] | Description |
|--------------------|-----|---------------------|--|
| TXD | 1 | I | transmit data input |
| GND ^[2] | 2 | G | ground |
| VCC | 3 | P | 5 V supply voltage input |
| RXD | 4 | O | receive data output |
| VIO | 5 | P | supply voltage input for I/O level adapter |
| SDO | 6 | I | SPI data output |
| INH | 7 | AO | inhibit output for switching external voltage supplies or indicating wake-up from Sleep mode (active-HIGH) |
| SCK | 8 | I | SPI clock input |
| WAKE | 9 | AI | local wake-up input |
| VBAT | 10 | P | battery supply voltage input |
| SDI | 11 | I | SPI data input |
| CANL | 12 | AIO | LOW-level CAN bus line |
| CANH | 13 | AIO | HIGH-level CAN bus line |
| SCSN | 14 | I | SPI chip select input (active-LOW) |

[1] I: digital input; O: digital output; AI: analog input; AO: analog output; AIO: analog input/output; P: power supply; G: ground.
[2] HVSON14 package die supply ground is connected to both the GND pin and the exposed center pad. The GND pin must be soldered to board ground. For enhanced thermal and electrical performance, it is also recommended to solder the exposed center pad to board ground.

Table 3. Pin description: TJA1445B

| Symbol | Pin | Type ^[1] | Description |
|--------------------|-----|---------------------|--|
| TXD | 1 | I | transmit data input |
| GND ^[2] | 2 | G | ground |
| VCC | 3 | P | 5 V supply voltage input |
| RXD | 4 | O | receive data output |
| VIO | 5 | P | supply voltage input for I/O level adapter |
| SDO | 6 | I | SPI data output |
| INH | 7 | AO | inhibit output for switching external voltage supplies or indicating wake-up from Sleep mode (active-HIGH) |
| GPIO3 | 8 | I/O | general purpose input/output 3 |
| TXEN_N | 9 | I | CAN transmitter enable/disable input (active-LOW) |
| SCK | 10 | I | SPI clock input |
| WAKE | 11 | AI | local wake-up input |
| VBAT | 12 | P | battery supply voltage input |
| SDI | 13 | I | SPI data input |
| CANL | 14 | AIO | LOW-level CAN bus line |
| CANH | 15 | AIO | HIGH-level CAN bus line |
| SCSN | 16 | I | SPI chip select input (active-LOW) |
| GPIO1 | 17 | I/O | general purpose input/output 1 |
| GPIO2 | 18 | I/O | general purpose input/output 2 |

[1] I: digital input; O: digital output; AI: analog input; AO: analog output; AIO: analog input/output; P: power supply; G: ground.

[2] DHVQFN18 package die supply ground is connected to both the GND pin and the exposed center pad. The GND pin must be soldered to board ground. For enhanced thermal and electrical performance, it is also recommended to solder the exposed center pad to board ground.

6 Functional description

6.1 Supply

Table 4. Supply description

| Supply | Description |
|------------------|---|
| V _{BAT} | Main supply for the device, needed for all internal processes; supplies the CAN receivers |
| V _{CC} | Supply for the CAN transmitter and for bus biasing |
| V _{IO} | Reference level for the digital interface pins TXD and RXD, the SPI interface, TXEN_N and the GPIO pins |

6.2 System operating modes

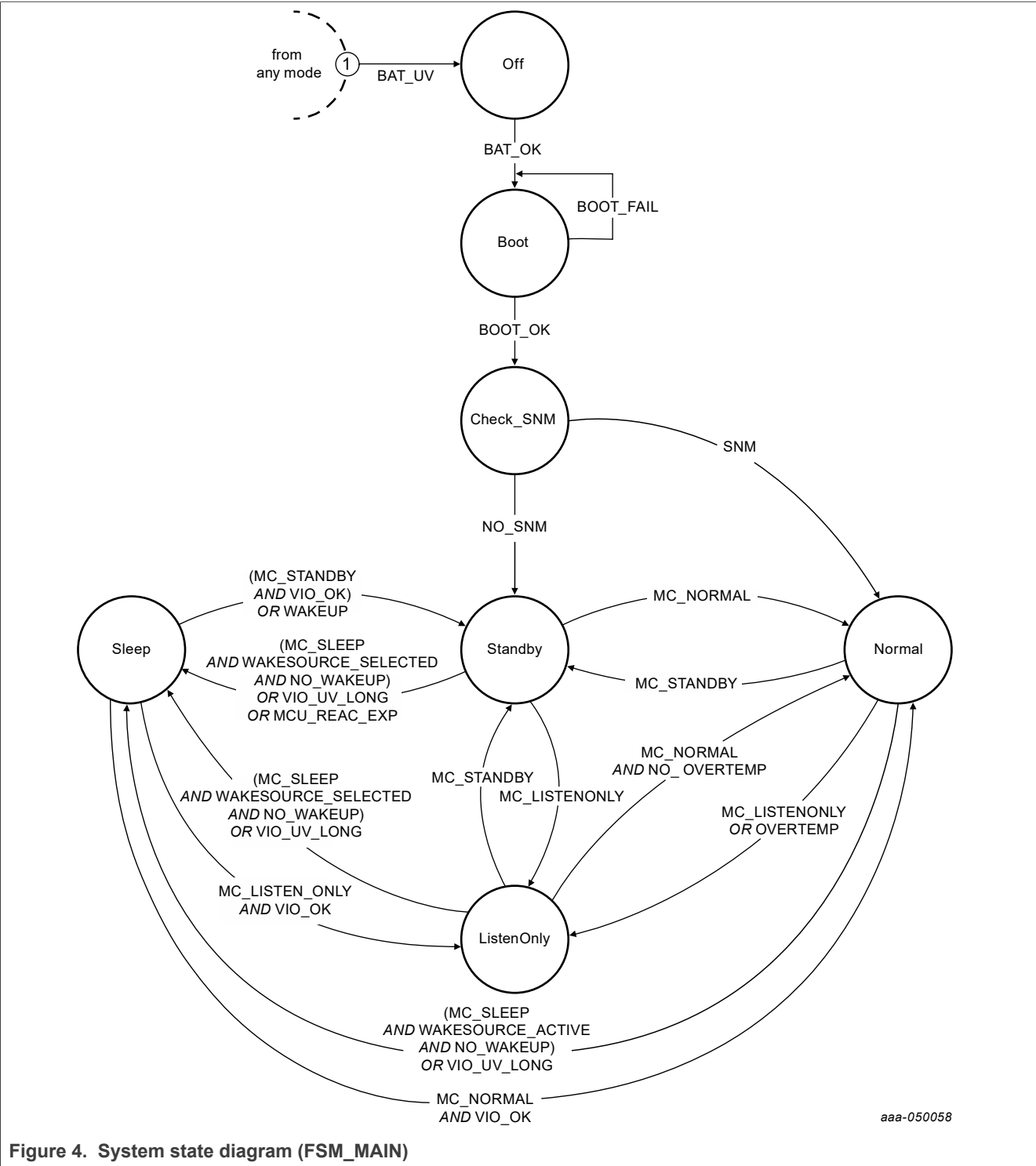
[Table 5](#) contains a summary of the system finite state machine (FSM_MAIN) operating modes. A mode transition diagram is shown in [Figure 4](#). Mode changes are completed after transition time $t_{t(moch)}$. Abbreviations used in the mode transition diagram are defined in [Table 6](#).

Table 5. FSM_MAIN operating modes

| Operating mode | Description |
|----------------|---|
| Off | The device switches to Off mode and is deactivated as a result of a low supply level on pin VBAT. |
| Boot | The device starts up and loads the configuration in Boot mode (it switches to Check_SNM mode after $t_{startup}$). |
| Check_SNM | The CAN bus is checked for a dominant state meeting Start-to-Normal mode (SNM) transition conditions. |
| Standby | Standby mode is the first-level low-power mode of the transceiver. |
| Sleep | Sleep mode is the second-level low-power mode of the transceiver. In this mode, pin INH is typically used to shut down the power supply to the host controller. Wake-up requests via the CAN bus or the local WAKE pin can be received in Sleep mode (if associated interrupts are enabled; see Table 35). |
| ListenOnly | In ListenOnly mode, only the CAN receiver is active. |
| Normal | Full transceiver and receiver capability is enabled in Normal mode. |

Table 6. State diagram legend

| Category | Abbreviation | Definition |
|--------------------------------|---------------------|---|
| VBAT pin status | BAT_UV | $V_{BAT} < V_{uvd}(VBAT)$ for $t > t_{det(uv)}VBAT$ |
| | BAT_OK | $V_{BAT} > V_{uvd}(VBAT)$ for $t > t_{rec(uv)}VBAT$ |
| Memory check during boot phase | BOOT_OK | passed internal memory consistency check |
| | BOOT_FAIL | failed internal memory consistency check |
| Start-to-Normal mode check | SNM | CAN bus must remain dominant for $t > t_{t(snm)}$ in Check_SNM mode; device switches to Normal mode (MC = Normal); SNMS = 1 |
| | NO_SNM | CAN bus recessive in CHECK_SNM mode; device switches to Standby mode (MC = Standby); SNMS = 0 |
| Wake-up request status | WAKEUP | valid local (WAKE) or remote (WUP/WUF) wake-up trigger received |
| | NO_WAKEUP | no valid local or remote wake-up trigger received |
| Wake-up source selection | WAKESOURCE_SELECTED | local (WAKE/GPIO) and/or remote wake-up source selected |
| Temperature status | NO_OVERTEMP | $T_j < T_{j(sd)rel}$ |
| | OVERTEMP | $T_j > T_{j(sd)}$ |
| VIO pin status | VIO_UV_LONG | $V_{IO} < V_{uvd}(VIO)$ for $t > t_{det(uv)long}$ |
| | VIO_OK | $V_{IO} > V_{uvd}(VIO)$ for $t > t_{rec(uv)}$ |
| MCU reaction timeout | MCU_REAC_EXP | no SPI activity for $t > t_{to}(MCU)$ |
| Mode select | MC_NORMAL | Normal mode (MC = 1111) |
| | MC_STANDBY | Standby mode (MC = 0110) |
| | MC_SLEEP | Sleep mode (MC = 0001) |
| | MC_LISTENONLY | ListenOnly mode (MC = 1000) |



In the state diagram, all transitions are mutually exclusive. A battery undervoltage overrides any transition, indicated by '1' (priority 1) in [Figure 4](#).

When the device powers up, the CAN bus is checked (in Check_SNM mode) for a bus dominant condition lasting longer than the start normal mode transition time ($t_{(snm)}$). When this condition is met (SNM), the devices switches to Normal mode, without the need for an SPI mode change command.

6.2.1 Pin and functional block states per operating mode

Table 7. Pin state per System operating mode

All supplies within operating range with no error condition present.

| Pin | Off/Boot/Check_SNM | Sleep | Standby | ListenOnly | Normal |
|---------------|----------------------------|--|--|----------------------------|----------------------------|
| TXD | high-Z | pull-up to V _{IO} | pull-up to V _{IO} | pull-up to V _{IO} | pull-up to V _{IO} |
| RXD | high-Z | V _{IO} or GND when interrupt pending ^[1] | V _{IO} or GND when interrupt pending ^[1] | CAN bus status | CAN bus status |
| SDO | high-Z | high-Z when SCSN HIGH | high-Z when SCSN HIGH | high-Z when SCSN HIGH | high-Z when SCSN HIGH |
| INH | high-Z | high-Z | V _{BAT} | V _{BAT} | V _{BAT} |
| SCK | high-Z | repeater | repeater | repeater | repeater |
| SDI | high-Z | repeater | repeater | repeater | repeater |
| SCSN | pull-up to V _{IO} | pull-up to V _{IO} | pull-up to V _{IO} | pull-up to V _{IO} | pull-up to V _{IO} |
| TJA1445B only | | | | | |
| GPIO1 | high-Z | GPIO | GPIO | GPIO | GPIO |
| GPIO2 | high-Z | GPIO | GPIO | GPIO | GPIO |
| GPIO3 | high-Z | GPIO | GPIO | GPIO | GPIO |
| TXEN_N | GND | pull-up to V _{IO} | pull-up to V _{IO} | pull-up to V _{IO} | pull-up to V _{IO} |

[1] Interrupt pending: at least one bit set in one or more interrupt status registers (see [Section 6.10.10](#)).

Table 8. Functional state per System operating mode

| Function | SPI configuration | Off/Boot/Check_SNM | Sleep | Standby | ListenOnly | Normal |
|------------------------|-------------------|--------------------|------------------------------|------------------------------|--------------------------|--------------------------|
| SPI | | off | on | on | on | on |
| CAN | | high-Z | GND or 2.5 V bias (autobias) | GND or 2.5 V bias (autobias) | 2.5 V bias and RX active | 2.5 V bias and TX active |
| Local wake-up | | off | on | on | on | on |
| CAN wake-up | PNCOK = 0 | off | on | on | off | off |
| | PNCOK = 1 | off | off | off | off | off |
| Partial networking | PNCOK = 0 | off | off | off | off | off |
| | PNCOK = 1 | off | on | on | on | on |
| Overtmp ^[1] | | off | off | off | off | on |

[1] Overtemperature detection remains active after a transition from Normal mode to ListenOnly mode due to an overtemperature condition.

6.2.2 Local wake-up via the WAKE pin

The device monitors the WAKE pin and can be configured to respond on a rising and/or falling edge:

- A WPR interrupt is generated on a rising edge if WPRE = 1 (see [Table 35](#))
- A WPF interrupt is generated on a falling edge if WPF = 1 (see [Table 35](#))

The wake-up detection filter time, the pulse width needed to trigger a wake-up event (t_{wake}), is configured via bit WFC in [Table 34](#). The WAKE pin status can be read via bit WPS in the System status register ([Table 16](#)). The GPIO pins on the TJA1445B can also be configured as V_{IO} level wake pins (see [Section 6.8](#)).

6.3 CAN operating modes

[Table 9](#) contains a summary of the CAN finite state machine (FSM_CAN) operating modes. A mode transition diagram is shown in [Figure 5](#). Abbreviations used in the mode transition diagram are defined in [Table 10](#).

Table 9. CAN operating modes

| Operating mode | Description |
|-----------------|--|
| CAN Off | The CAN transceiver is disconnected from the bus (high-Z) |
| CAN Offline | The CAN transceiver is in a low-power mode, able to react to a wake-up pattern (WUP) on the bus |
| CAN OfflineBias | The CAN transceiver is in a low-power mode, able to react to a wake-up pattern (WUP) or wake-up frame (WUF) on the bus |
| CAN ListenOnly | Only the CAN receiver is active, the RXD pin reflects the CAN bus status and is able to capture a wake-up frame (WUF) |
| CAN Active | The CAN transceiver is active and able to capture a wake-up frame (WUF). |

Table 10. State diagram legend

| Category | Abbreviation | Definition |
|----------------|--------------|---|
| CAN bus events | BUSSILENCE | CAN bus idle for $t > t_{to(silence)}$ |
| | WUP | valid CAN wake-up pattern detected |
| VCC pin status | VCC_OK | $V_{CC} > V_{uvd(VCC)}$ for $t > t_{rec(uv)}$ |
| | VCC_UV | $V_{CC} < V_{uvd(VCC)}$ for $t > t_{det(uv)}$ |

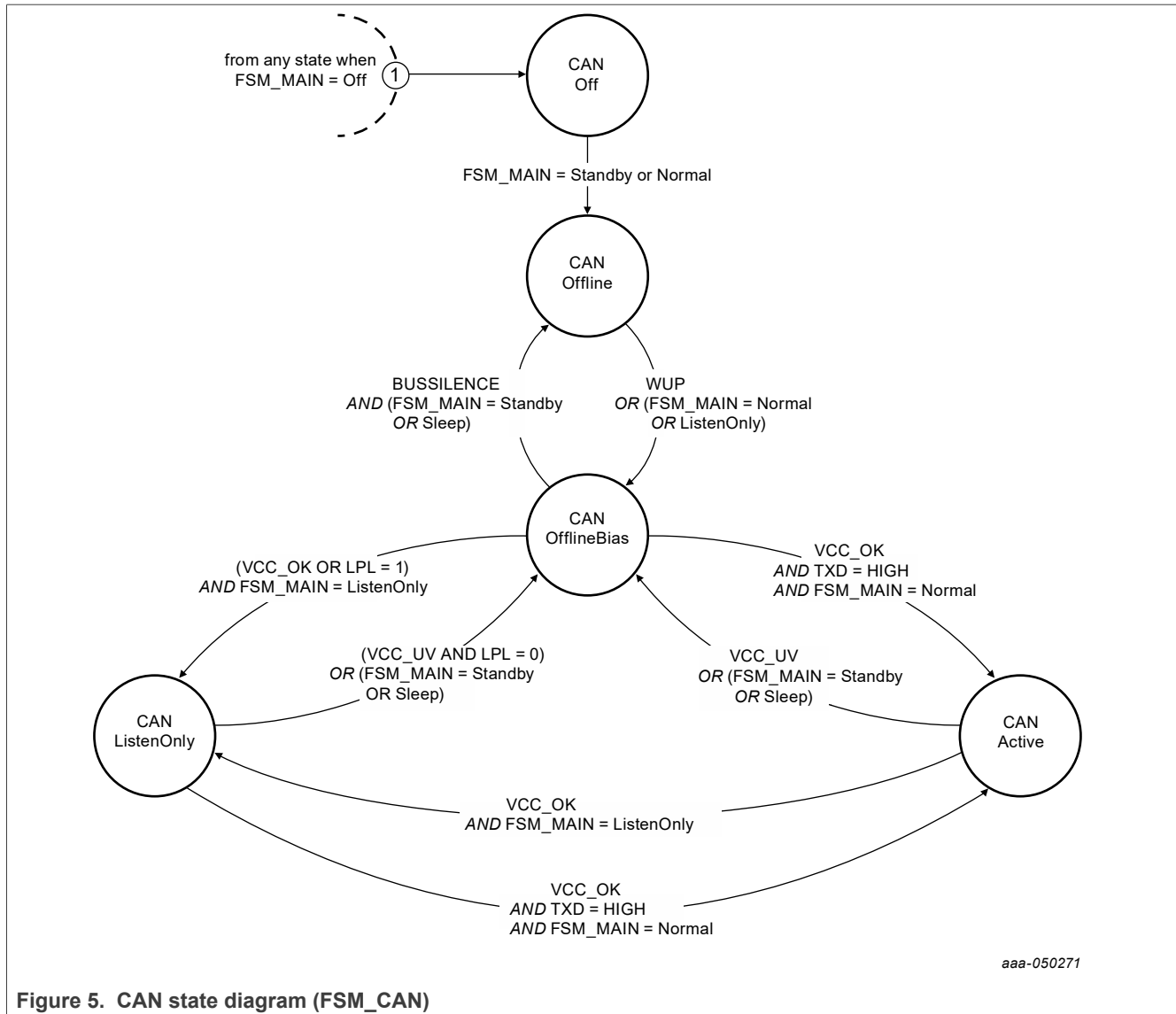


Figure 5. CAN state diagram (FSM_CAN)

State transitions are mutually exclusive. An FSM_MAIN = Off condition overrides any state transition, indicated by '1' (priority 1) in Figure 5.

Low-power ListenOnly mode (LPL = 1; see Figure 5 and Table 18) is intended for Pretended Networking use cases and provides CAN listen-only behavior without a V_{CC} supply. In this mode, the CAN transmitter is switched off to minimize quiescent current and CAN bus biasing is derived from V_{BAT} (see Table 11). The receiver operates normally.

6.3.1 Functional block state per CAN operating mode

Table 11. Functional block state per CAN operating mode

| Block | SPI configuration | CAN Off | CAN Offline | CAN Offline Bias | CAN Listen Only | CAN Active |
|-----------------|-------------------|---------|-------------|------------------|-----------------|-----------------------|
| CAN transmitter | LPL = 0 | off | off | off | recessive | active ^[1] |
| | LPL = 1 | off | off | off | off | active ^[1] |
| CAN receiver | | off | off | off | active | active |

Table 11. Functional block state per CAN operating mode...continued

| Block | SPI configuration | CAN Off | CAN Offline | CAN Offline Bias | CAN Listen Only | CAN Active |
|----------|-------------------------|---------|-------------|------------------------------|------------------------------|------------|
| CAN bias | VBATVCC = 1 | high-Z | GND | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ |
| | LPL = 0 and VBATVCC = 0 | high-Z | GND | 2.5 V derived from V_{BAT} | $V_{CC}/2$ | $V_{CC}/2$ |
| | LPL = 1 and VBATVCC = 0 | high-Z | GND | 2.5 V derived from V_{BAT} | 2.5 V derived from V_{BAT} | $V_{CC}/2$ |

[1] If TXEN_N is HIGH in TJA1445B, status will be recessive

6.3.2 CAN wake-up

The TJA1445 supports remote wake-up via a CAN wake-up pattern (WUP) or selective wake-up via a CAN wake-up frame (WUF).

6.3.2.1 CAN wake-up pattern (WUP)

The CAN wake-up pattern (WUP) is used for two purposes:

- To activate CAN biasing in CAN Offline mode (transition from CAN offline to CAN OfflineBias)
- To trigger a CAN wake-up event

The following conditions must be met to trigger a wake-up event via a CAN WUP:

- The CAN transceiver is in CAN Offline or CAN OfflineBias mode
- CAN wake-up enabled (CWE = 1)
- CAN wake-up frame detection (WUF) deactivated (CPNC = 0 or PNCOK = 0)

The TJA1445 supports both the standard (ISO11898-2:2016) and the extended (anticipated from the ISO11898-2:2023 update) wake-up patterns (see [Figure 6](#) and [Figure 7](#)). The WUP is selected via bit CWC in the CAN configuration register ([Table 18](#)).

The wake-up pattern consists of:

[ISO11898-2:2016 standard WUP]

- a dominant phase of at least $t_{wake(busdom)}$ followed by
- a recessive phase of at least $t_{wake(busrec)}$ followed by
- a dominant phase of at least $t_{wake(busdom)}$

[ISO11898-2:2023 WUP extension]

- followed by a recessive phase of at least $t_{wake(busrec)}$

Dominant or recessive bits between the phases shorter than $t_{wake(busdom)}$ or $t_{wake(busrec)}$, respectively, are ignored.

The complete dominant-recessive-dominant (standard WUP) or dominant-recessive-dominant-recessive (WUP extension) pattern must be received within $t_{to(wake)bus}$ to be recognized as a valid wake-up pattern (see [Figure 6](#) and [Figure 7](#)). Otherwise, the internal wake-up logic is reset. The complete wake-up pattern then needs to be retransmitted to trigger a wake-up event.

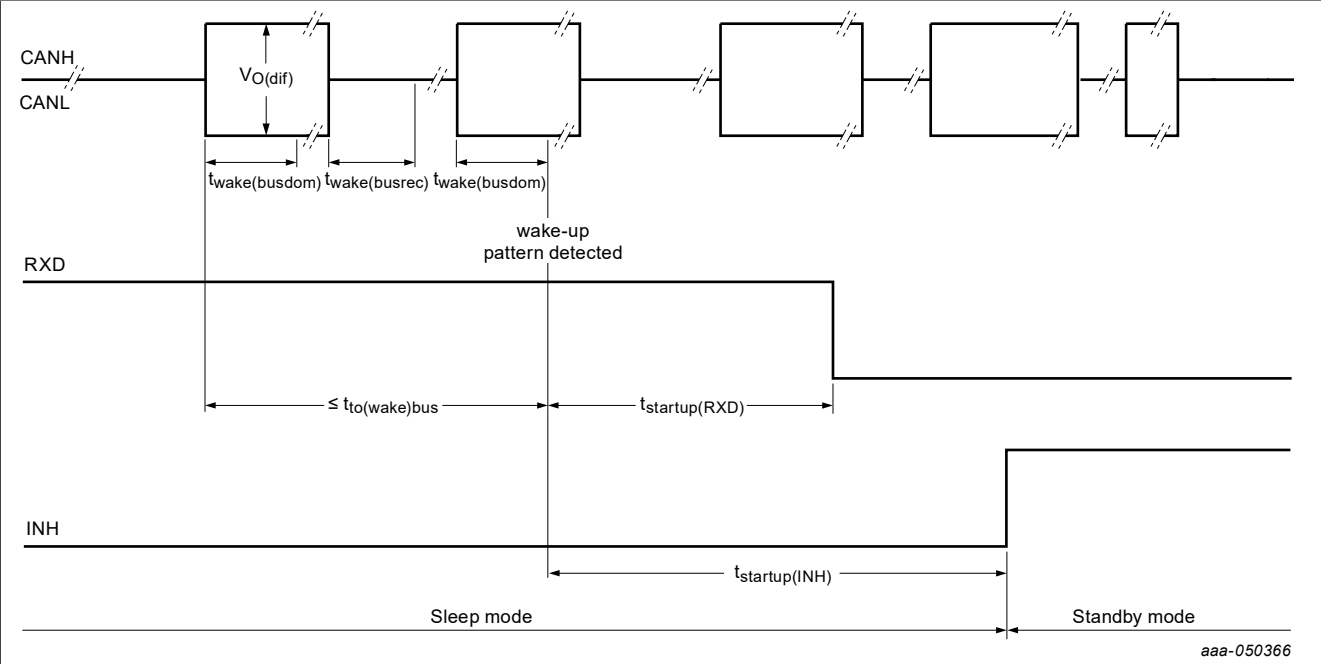


Figure 6. Standard wake-up pattern in Sleep mode with $CWE = 1$, $PNCOK = 0$ and $CWC = 0$

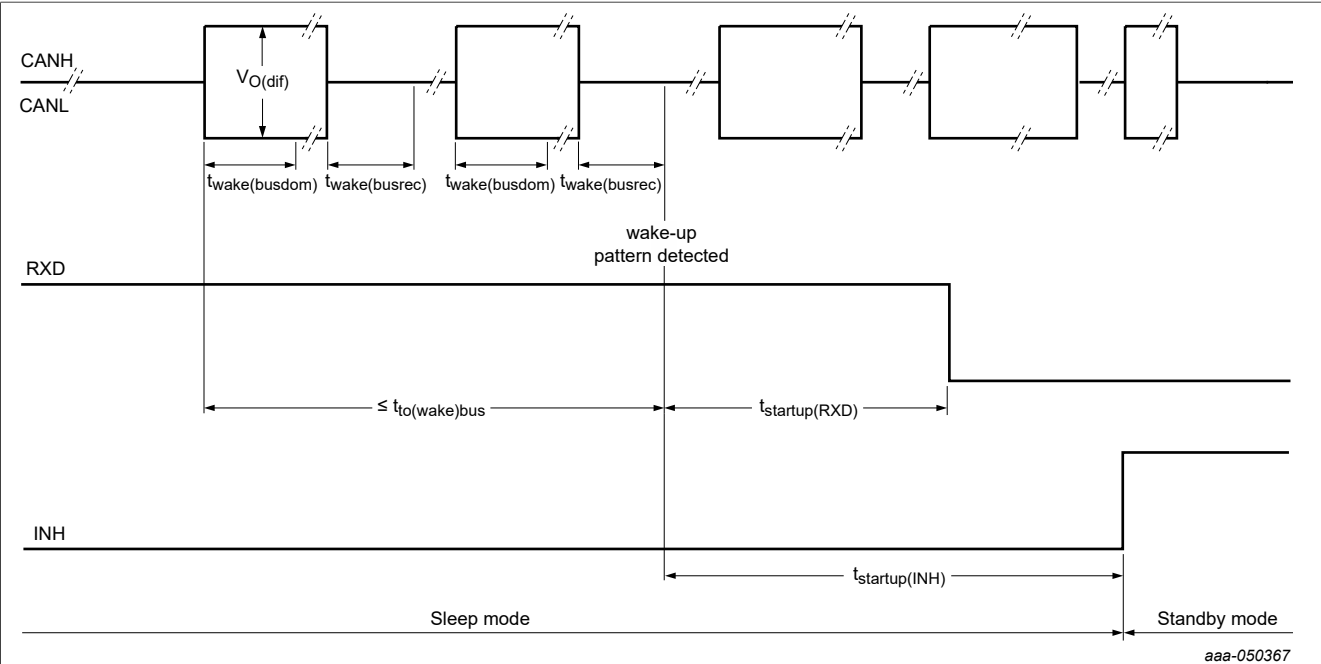


Figure 7. Extended wake-up pattern in Sleep mode with $CWE = 1$, $PNCOK = 0$ and $CWC = 1$

6.3.2.2 CAN wake-up frame (WUF)

CAN partial networking through selective wake-up detection allows a device in a CAN network to be selectively woken up in response to a dedicated wake-up frame (WUF) on the CAN bus.

Selective wake-up detection uses one of two filtering methods:

- Identifier-only filtering (PNDM = 0)
- Identifier + data mask filtering (PNDM = 1)

The following conditions must be met to enable CAN WUF functionality:

- The FSM_CAN is in CAN OfflineBias, CAN ListenOnly, or CAN Active mode
- CAN wake-up enabled (CWE = 1)
- CAN partial networking configured correctly (PNCOK = 1)
- CAN partial networking enabled (CPNC = 1)
- No CAN partial networking error detected (CPNERRS = 0)

The TJA1445 clears PNCOK after a further write access to one or more of the CAN partial networking configuration registers:

- Partial networking data rate and filter configuration register ([Table 31](#))
- Partial networking frame control register ([Table 30](#))
- Partial networking data mask registers ([Table 29](#))
- Partial networking ID registers ([Table 27](#))
- Partial networking ID mask registers ([Table 28](#))
- Partial networking and CAN configuration register ([Table 32](#))

Storing a new configuration involves multiple write cycles to the registers; setting PNCOK signals to the device that the configuration has been loaded.

The arbitration bit rate is selected via bits CDR (see [Table 31](#)). CAN bit rates of 50 kbit/s, 100 kbit/s, 125 kbit/s, 250 kbit/s, 500 kbit/s, 667 kbit/s and 1000 kbit/s are supported during selective wake-up.

6.3.2.2.1 Identifier matching

The wake-up frame format, standard (11-bit) or extended (29-bit) identifier, is selected via bit IDE in the frame control register ([Table 30](#)).

- IDE = 0: standard CBFF (classical base frame format, 11-bit)
- IDE = 1: extended CEFF (classical extended frame format, 29-bit)

A valid WUF identifier is defined and stored in the ID registers ([Table 27](#)). An ID mask can be defined to exclude selected bits from being evaluated during WUF detection. The ID mask is defined in the mask registers ([Table 28](#)), where a 1 means 'don't care'.

When PNDM = 0, a valid wake-up frame is detected and a wake-up event is captured (CAN wake-up interrupt generated; see [Table 38](#)) when:

- the identifier field in the received wake-up frame matches the pattern in the ID registers (excluding the masked bits)
- the frame is a valid CBFF or CEFF frame according to the ISO 11898-1:2016 (including CRC and CRC delimiter)

6.3.2.2.2 Data field matching

In addition to the identifier field, the data field in the CAN frame is also evaluated during WUF detection when $PNDM = 1$.

The data field indicates the nodes to be woken up. Within the data field, groups of nodes can be pre-defined and associated with bits in a data mask. By comparing the incoming data field with the data mask, multiple groups of nodes can be woken up simultaneously with a single wake-up message.

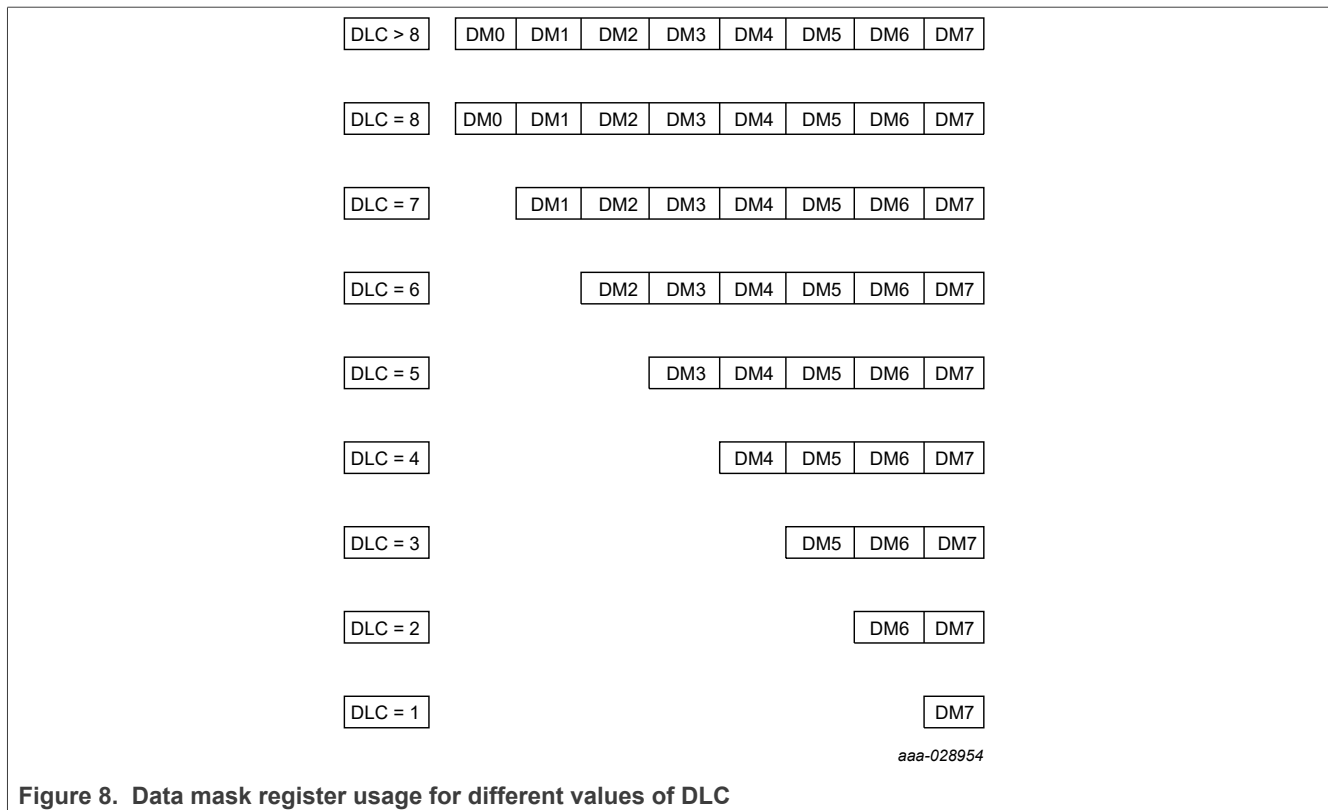
The data length code (bits DLC in the frame control register; [Table 30](#)) determines the number of data bytes expected (between 0 and 8) in the data field of a CAN wake-up frame. If one or more data bytes are expected ($DLC \neq 0000$), at least one bit in the data field of the received wake-up frame must be set to 1 and at least one equivalent bit in the associated data mask register in the transceiver (see [Table 29](#)) must also be set to 1 for a successful wake-up. Each matching pair of 1s indicates a group of nodes to be activated (since the data field is up to 8 bytes long, up to 64 groups of nodes can be defined).

If $DLC = 0000$, a node will wake up if the WUF contains a valid identifier and the received data length code is 0000, regardless of the values stored in the data mask (the data field is not evaluated when $DLC = 0000$). If $DLC \neq 0000$ and all data mask bits are set to 0, the device cannot be woken up via the CAN bus (note that all data mask bits are set to 1 by default; see [Table 29](#)). If a WUF contains a valid ID but the DLCs (in the Frame control register and in the WUF) don't match, the data field is ignored and no nodes are woken up.

Remote frames do not contain data, but request data and can have a $DLC \neq 0000$; so remote frames are not supported when $PNDM = 1$. If remote frames need to trigger a wake-up, identifier-only filtering should be selected ($PNDM = 0$).

When $PNDM = 1$, a WUF is detected when the following conditions are met:

- The identifier field in the received wake-up frame matches the pattern and format in the ID registers ([Table 27](#)), excluding masked bits.
- The received CAN frame is not a Remote frame.
- The received data length code matches the DLC setting in the frame control register ([Table 30](#)).
- $DLC \neq 0000$ and at least one bit in the data field of the received frame is set with the corresponding bit in the associated data mask register ([Table 29](#)) also set.
- The frame is a valid CBFF or CEFF frame according to the ISO 11898-1:2016 (including CRC and CRC delimiter).



6.3.2.2.3 WUF error processing

If the TJA1445 receives a CAN message containing a protocol error (e.g. a 'stuffing error') transmitted in advance of the ACK field, an internal error counter is incremented. If a classical CAN message (CBFF or CEFF) is received without any errors appearing in front of the ACK field, the counter is decremented. Data received after the CRC delimiter and before the next SOF is ignored by the CAN wake-up frame detector module. If the counter overflows (counter > 31), a frame detect error is captured (PNFDER = 1) and the device wakes up.

The error counter value can be read via bits PN_ERR_ERROR_COUNT ([Table 26](#)). The counter is reset to zero when no activity is detected on the CAN bus for $t_{to(silence)}$ or selective wake-up detection is disabled (CPNC = 0 OR PNCOK = 0). The status, whether the last frame was decoded successfully, can be determined via bit LFDS in the partial networking status register ([Table 25](#)).

If selective wake-up is disabled (CPNC = 0) or partial networking is not configured correctly (PNCOK = 0), wake-up will be performed as described in [Section 6.3.2.1](#).

6.3.2.2.4 CAN FD passive

CAN frames in the ISO 11898-1:2016 compliant FD base frame format (FBFF) or FD extended frame format (FEFF) are not supported for selective wake-up. The device can be configured to tolerate these frames or treat them as invalid frames via bit PNECC in the partial networking control register ([Table 32](#)).

With PNECC = 0, the error counter is incremented when an FBFF or FEFF frame is received. FBFF and FEFF frames are ignored when PNECC = 1 and the error counter is not affected.

CAN FD tolerance is supported as described in the ISO11898-2, bit filter 1 and 2 standard. The TJA1445 also supports additional bit filter settings for higher data rates up to 8 Mbit/s (see bit IDFS in [Table 31](#)).

6.4 Interrupt processing

A number of events can be captured and reported to the host via the interrupt mechanism. Pin RXD is used to signal an interrupt event in Standby or Sleep mode. Two options are supported:

- RXDINTC = 0: RXD goes LOW when a wake-up or power-on interrupt is pending
- RXDINTC = 1: RXD goes LOW when any interrupt is pending

Interrupts are enabled individually via dedicated bits in the interrupt enable registers (see [Section 6.10.10](#)). When an interrupt is generated, pin RXD goes LOW to alert the host. The host can then determine which event triggered the interrupt by polling the interrupt status registers. PO and PNFDER interrupts are always enabled; so they do not have associated interrupt enable bits.

Interrupts are cleared by writing 1 (W1C) to the relevant interrupt status bits. Clearing an interrupt does not necessarily mean the event that triggered the interrupt has been resolved. If there is a collision, setting the interrupt takes precedence over clearing the interrupt.

6.5 Device ID

A byte is reserved in the register map for the unique device identification code; see bit IDS in [Table 44](#).

6.6 Lock control

Sections of the register address area can be write-protected to prevent unintended modifications. Note that this facility only protects locked bits from being modified via the SPI and will not prevent the TJA1445 updating registers. Sections that can be locked are detailed in [Section 6.10.11](#).

6.7 General-purpose memory

The TJA1445 allocates 4 bytes of memory to store user information. The general-purpose registers can be accessed via the SPI at address 0xFF0 to 0xFF3 (see [Section 6.10.12](#)). The general-purpose registers are only cleared when the battery is first connected.

6.8 GPIO pins - TJA1445B only

The TJA1445B contains three configurable general-purpose I/O pins that can be assigned to a number of functions (see [Table 22](#), [Table 23](#) and [Table 24](#)).

The GPIOs can be individually configured as digital input, output or inactive (repeater) pins:

- input options: floating, pull-up, pull-down or repeater
- output options:
 - push-pull
 - open-drain high-side driver
 - high-side driver plus weak pull-down
 - open-drain low-side driver
 - low-side driver plus weak pull-up

For a number of functions, the GPIO pins can be configured as active-HIGH or active-LOW, selected via bits GPPx in [Table 20](#).

Table 12. Configurable GPIO functions

| GPIO function | Description |
|-----------------------------------|-------------|
| Digital input, output or inactive | - |

Table 12. Configurable GPIO functions ...continued

| GPIO function | Description |
|--|---|
| TXEN_N input | CAN transmitter disabled when GPIO pin driven HIGH |
| INT_N interrupt output | active-LOW by default (GPPx = 0); LOW signals an interrupt is pending |
| Additional RXD output (RXD2) | GPIO1 only, two options: <ul style="list-style-type: none"> CAN bus forwarded to both RXD and RXD2 (via GPIO1) outputs CAN bus forwarded to RXD2 only; RXD forced HIGH |
| Additional TXD digital interface (TXD2) | GPIO2 only, two options: <ul style="list-style-type: none"> TXD and TXD2 (via GPIO2) data fed to the CAN bus - the CAN bus will be recessive only when both TXD and TXD2 are HIGH only TXD2 enabled (TXD input ignored) - the CAN bus is driven dominant when TXD2 is LOW |
| V _{CC} undervoltage status output | active-HIGH by default (configurable via GPPx), HIGH indicates V _{CC} undervoltage detected (UVCCS) |
| TXD dominant status output | active-HIGH by default (configurable via GPPx), HIGH indicates TXD clamped dominant (TXDDOMS) |
| TXD2 dominant status output | active-HIGH by default (configurable via GPPx), HIGH indicates TXD2 clamped dominant (TXD2DOMS) - GPIO1 and GPIO3 only |
| CAN WUP detect status output | active-HIGH by default configurable via GPPx, HIGH indicates WUP detected |
| CAN WUF detect status output | active-HIGH by default (configurable via GPPx), HIGH indicates WUF detected |
| CAN bus biasing status output | active-HIGH by default (configurable via GPPx), HIGH indicates bus biasing is active |
| WAKE pin rising edge detect output | active-HIGH by default (configurable via GPPx), HIGH indicates rising edge detected on WAKE pin |
| WAKE pin falling edge detect output | active-HIGH by default (configurable via GPPx), HIGH indicates falling edge detected on WAKE pin |
| CAN in Active mode and ready to transmit status output (CTS) | active-HIGH by default (configurable via GPPx), HIGH if CAN in Active mode |
| CAN in ListenOnly mode status output | active-HIGH by default (configurable via GPPx), HIGH if CAN in ListenOnly mode |
| Low-voltage wake-up input | wake-up on rising, falling or both edges on GPIO pin |
| INH2: low-voltage inhibit output | active-HIGH by default (configurable via GPPx), HIGH if INH2 activated |

The status of the GPIO pins, HIGH or LOW, can be read via bits GPIOxS in the GPIO status register ([Table 21](#)).

6.9 Failure handling

The TJA1445 incorporates a number of safety features used for error detection and processing.

6.9.1 TXD dominant timeout

A LOW level on pin TXD (or on GPIO2 in TJA1445B when configured as a second TXD input, see [Section 6.8](#)) persisting longer than $t_{to(dom)TXD}$ releases the bus lines to recessive state. This feature prevents the CAN bus being blocked by continuous dominant clamping. A CAN failure interrupt is generated (TXDDOM/TXD2DOM = 1), if enabled (TXDDOME/TXD2DOME = 1), when a TXD dominant timeout is detected. The TXD dominant status can be read via bit TXDDOMS/TXD2DOMS in the CAN status register ([Table 19](#)).

6.9.2 CAN transmitter enable/disable(TXEN_N) - TJA1445B only

On the TJA1445B, the CAN transmitter can be enabled/disabled via the TXEN_N input. The GPIO pins can be configured as additional transmitter enable/disable signals (see [Section 6.8](#)). A HIGH level on pin TXEN_N, or on a GPIO pin configured as a TXEN_N input, disables the transmitter, releasing the bus lines to recessive state independent of the level on pin TXD and/or TXD2 (if configured on GPIO2). The TXEN_N status can be read via bit GPIO1S, GPIO2S and GPIO3S in the GPIO status register ([Table 21](#)).

6.9.3 Bus dominant timeout

A dominant state on the CAN bus lasting longer than $t_{to(dom)bus}$ generates a CAN bus failure interrupt (BUSDOM = 1), if enabled (BUSDOME = 1; [Table 36](#)). The status of the bus can be read via bit BUSDOMS in the CAN status register ([Table 19](#)). Note that this feature is only available in Normal mode and in Listen Only modes when LPL = 0.

6.9.4 V_{BAT} undervoltage

The TJA1445 monitors the supply voltage on pin VBAT. It switches directly to Off mode when V_{BAT} drops below the undervoltage detection threshold, V_{uvd(VBAT)} for $t_{det(uv)}$. As a consequence, bit PO is set (see [Table 38](#)).

6.9.5 V_{IO} undervoltage

The TJA1445 monitors the supply voltage on pin VIO. When V_{IO} drops below the undervoltage detection threshold V_{uvd(VIO)} for longer than $t_{det(uv)long}$, the device switches to Sleep mode and the wake-up sources (CWE, WPRE and WPFE) are enabled automatically. A long VIO undervoltage interrupt is generated (LUVIO = 1), if enabled (LUVIOE = 1; see [Table 16](#)). On recovering from an undervoltage event, the TJA1445 switches back to the selected mode (MC). Note that a long undervoltage event on VIO (LUVIO) will not be captured in Sleep mode.

The long undervoltage detection time, $t_{det(uv)long}$, is selected via bit LUVIOSEL in the system configuration register ([Table 17](#)).

6.9.6 V_{CC} undervoltage

The TJA1445 monitors the supply voltage on pin VCC. When V_{CC} drops below the undervoltage detection threshold V_{uvd(VCC)} for longer than $t_{det(uv)}$, a V_{CC} undervoltage interrupt is generated (UVCC = 1), if enabled (UVCCE = 1; [Table 35](#)). The V_{CC} undervoltage status can be read via bit UVCCS in the system status register ([Table 16](#)).

6.9.7 Overtemperature

The TJA1445 monitors the junction temperature. When the junction temperature exceeds $T_{j(sd)}$, the device switches from Normal mode to ListenOnly mode (see [Figure 1](#)). An overtemperature interrupt is generated (OT = 1), if enabled (OTE = 1; see [Table 38](#)). The device recovers and switches back to Normal mode when the junction temperature falls below the shutdown release threshold, $T_{j(sd)rel}$. The overtemperature status can be read via bit OTS in the system status register ([Table 16](#)) when the device is in Normal or ListenOnly mode.

6.9.8 MCU reaction timeout

When the TJA1445 enters Standby mode from Boot or Sleep mode, the MCU reaction timeout timer is started. If a valid SPI frame is not detected within $t_{to(MCU)}$, the device switches to Sleep mode and waits for a wake-up request.

The MCU reaction timeout time depends on the long undervoltage threshold, selected via bit LUVIOSEL in the system configuration register ([Table 17](#) and [Table 48](#)).

6.10 SPI interface

The serial peripheral interface (SPI) provides the communication link with the microcontroller. The SPI is configured for full duplex data transfer, so status information is returned when new control data is shifted in. The interface also offers a read-only access option, allowing registers to be read back by the application without changing the register content.

The SPI uses four interface signals for synchronization and data transfer:

- SCSN: SPI chip select; active LOW
- SCK: SPI clock
- SDI: SPI data input
- SDO: SPI data output; floating when pin SCSN is HIGH (may need external pull-up or pull-down if not available in the host controller)

Bit sampling is performed on the falling edge of the clock and data is shifted in/out on the rising edge, as illustrated in [Figure 9](#).

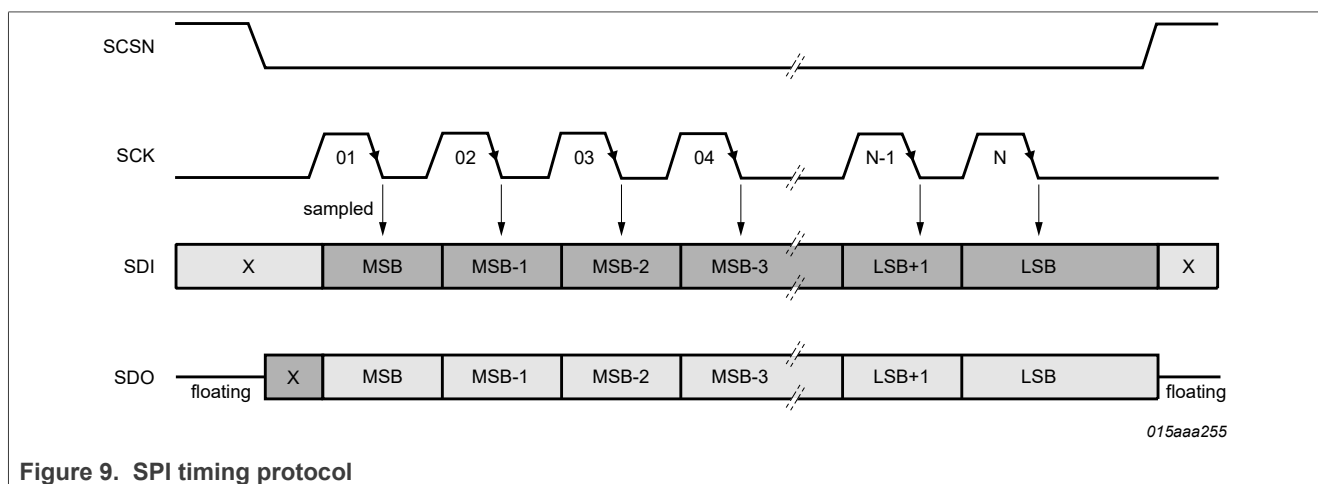


Figure 9. SPI timing protocol

The SPI data in the TJA1445 is stored in a number of dedicated 8-bit registers. Each register is assigned a unique 12-bit address. A minimum of three bytes (24 bits) must be transmitted to the TJA1445 for a single register read or write operation (see [Figure 9](#)). Six bytes (48 bits) are needed to transmit the maximum of 4 data bytes.

The first byte contains the 8 most significant bits of the address; the second byte contains the 4 least significant bits of the address, a 'read-only' bit, a 2-bit payload size (PLS) and a parity bit. The read-only bit must be 0 to indicate a write operation and 1 to indicate a read operation. PLS indicates the number of data bytes being transmitted:

- 00 - 1 data byte
- 01 - 2 data bytes
- 10 - 3 data bytes
- 11 - 4 data bytes

The parity bit covers the address bits, read-only bit and PLS bits. It must be calculated in the user application as part of the SPI command indicating even parity, creating an even number of 1s in the first 2 bytes including the parity bit.

The third and subsequent bytes contain the data to be written. For two or more data bytes (PLS \neq 00), the register address is incremented automatically after each data byte, see [Figure 10](#).

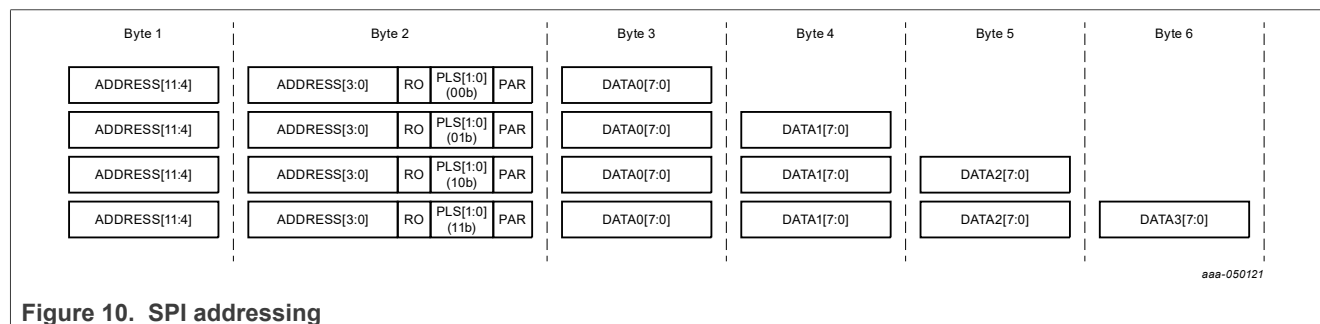


Figure 10. SPI addressing

During the SPI data, read or write operation, the first 15 bits received on pin SDI are returned via pin SDO; bit 16 returns the parity calculated for these 15 bits. During the data phase of the SPI protocol, the contents of the addressed register is returned via the SDO pin.

The device tolerates attempts to write to registers that do not exist.

6.10.1 SPI error handling

The TJA1445 can detect a number of SPI transmission failures:

- an incorrect parity bit was received
- the number of clock cycles is less than 24 or does not match the expected value based on the PLS
- an address rollover ($> 0xFFFF$) was detected
- an undefined MC code was received
- a write access was attempted to a locked register
- an illegal sleep command was received (no wake-up source enabled)
- the SPI message was not completed (SCSN HIGH) within the timeout time, $t_{to}(SPI)$

In all cases, an SPI fail interrupt is generated.

In the case of an incorrect parity or too many clock cycles, pin SDO goes LOW until the next rising edge on SCSN. When the duration of the SPI message exceeds $t_{to}(SPI)$, the SDO pin goes high-Z.

6.10.2 SPI system reset

A system reset can be forced via the SPI, causing the device to restart via Boot mode. A system reset is initiated by writing, consecutively, 0x01 then 0x80 to bits SFR in the system reset register (see [Table 33](#)). Both SPI accesses should be 24-bit. Any deviation from this sequence will abort the system reset.

Information that was in the general-purpose memory ([Table 43](#)) when the reset was initiated will still be available after the reset sequence has been completed.

6.10.3 SPI register map

Table 13. SPI register map overview

| Register type | Address | Register name |
|--------------------|---------|--|
| Mode control | 0x000 | Mode control register |
| Interrupt enable | 0x010 | System interrupt enable register |
| | 0x011 | CAN interrupt enable register |
| | 0x012 | GPIO interrupt enable register - TJA1445B only |
| Partial networking | 0x020 | Partial networking ID register 0 |
| | 0x021 | Partial networking ID register 1 |
| | 0x022 | Partial networking ID register 2 |
| | 0x023 | Partial networking ID register 3 |
| | 0x024 | Partial networking ID mask register 0 |
| | 0x025 | Partial networking ID mask register 1 |
| | 0x026 | Partial networking ID mask register 2 |
| | 0x027 | Partial networking ID mask register 3 |
| | 0x028 | Partial networking data mask register 0 |
| | 0x029 | Partial networking data mask register 1 |
| | 0x02A | Partial networking data mask register 2 |
| | 0x02B | Partial networking data mask register 3 |
| | 0x02C | Partial networking data mask register 4 |
| | 0x02D | Partial networking data mask register 5 |
| | 0x02E | Partial networking data mask register 6 |
| | 0x02F | Partial networking data mask register 7 |
| | 0x030 | Partial networking frame control register |
| | 0x031 | Partial networking data rate and filter configuration register |
| | 0x032 | Partial networking and CAN configuration register |
| Configuration | 0x040 | Wake-up pulse configuration register |
| | 0x041 | CAN configuration register |
| | 0x042 | GPIO1 configuration register - TJA1445B only |
| | 0x043 | GPIO2 configuration register - TJA1445B only |
| | 0x044 | GPIO3 configuration register - TJA1445B only |
| | 0x045 | GPIO polarity configuration register - TJA1445B only |
| | 0x046 | System configuration register |
| Lock | 0x050 | Lock control register |
| Interrupt status | 0x060 | System interrupt status register |
| | 0x061 | CAN interrupt status register |
| | 0x062 | Partial networking interrupt status register |
| | 0x063 | GPIO interrupt status register - TJA1445B only |

Table 13. SPI register map overview...continued

| Register type | Address | Register name |
|------------------------|---------|--|
| General status | 0x070 | Mode status register |
| | 0x071 | System status register |
| | 0x072 | CAN status register |
| | 0x073 | Partial networking status register |
| | 0x074 | GPIO/TXEN_N status register - TJA1445B only |
| | 0x075 | Partial networking error count status register |
| Reset | 0xFE0 | System reset register |
| General-purpose memory | 0xFF0 | General-purpose memory register 0 |
| | 0xFF1 | General-purpose memory register 1 |
| | 0xFF2 | General-purpose memory register 2 |
| | 0xFF3 | General-purpose memory register 3 |
| ID | 0xFFF | Device identification |

6.10.4 System control and status registers

Reset values are indicated by '*'.

Table 14. Mode control register (address 000h)

| Bit | Symbol | Access | Value | Description |
|-----|----------|--------|-------|-----------------------------------|
| 7:4 | reserved | R | - | always write 0000; ignore on read |
| 3:0 | MC | R/W | 0001 | Sleep mode |
| | | | 0110* | Standby mode |
| | | | 1000 | ListenOnly mode |
| | | | 1111 | Normal mode |

Table 15. Mode status register (address 070h)

| Bit | Symbol | Access | Value | Description |
|-----|----------|--------|-------|-----------------|
| 7:4 | reserved | R | - | ignore on read |
| 3:0 | MCS | R | 0001 | Sleep mode |
| | | | 0110 | Standby mode |
| | | | 1000 | ListenOnly mode |
| | | | 1111 | Normal mode |

Table 16. System status register (address 071h)

| Bit | Symbol | Access | Value | Description |
|-----|----------|--------|-------|----------------|
| 7 | reserved | R | - | ignore on read |

Table 16. System status register (address 071h)...continued

| Bit | Symbol | Access | Value | Description |
|-----|----------|--------|-------|---|
| 6 | FSMS | R | | most recent Sleep mode transition: |
| | | | 0 | triggered by SPI |
| | | | 1 | triggered by VIO undervoltage or MCU timeout |
| 5 | OTS | R | | overtemperature status available when MC = Normal and MCS = Normal/Listen Only |
| | | | 0 | no overtemperature or MC ≠ Normal |
| | | | 1 | overtemperature detected |
| 4 | reserved | R | - | ignore on read |
| 3 | UVCCS | R | | V _{CC} undervoltage status |
| | | | 0 | no undervoltage on VCC |
| | | | 1 | V _{CC} undervoltage detected |
| 2 | NMS | R | | Normal mode status |
| | | | 0 | device entered Normal mode after power up |
| | | | 1 | device did not enter Normal mode power up |
| 1 | SNMS | R | | Start-to-Normal mode status |
| | | | 0 | device did not enter Normal mode after power up (bus dominant for $t < t_{(snm)}$ or recessive; NO_SNM) |
| | | | 1 | device entered Normal mode after power up due to CAN bus clamped dominant (SNM) |
| 0 | WPS | R | | WAKE pin status |
| | | | 0 | WAKE pin LOW |
| | | | 1 | WAKE pin HIGH |

Table 17. System configuration register (address 046h)

| Bit | Symbol | Access | Value | Description |
|-----|----------|--------|-------|---|
| 7:4 | reserved | R | - | always write 0000; ignore on read |
| 3 | BCCTRL | R/W | | V _{BAT} clamp control: |
| | | | 0* | enable V _{BAT} clamp |
| | | | 1 | disable V _{BAT} clamp |
| 2 | RXDINTC | R/W | | interrupt signaling at RXD in Sleep/Standby modes |
| | | | 0* | wake-up and power-on interrupts detected |
| | | | 1 | all enabled interrupts detected |
| 1 | LUVIOSEL | R/W | | long VIO undervoltage detection time select: |
| | | | 0 | $t_{det(uv)long1}$ |
| | | | 1* | $t_{det(uv)long2}$ |
| 0 | VBATVCC | R/W | | VBAT/VCC configuration |

Table 17. System configuration register (address 046h)...continued

| Bit | Symbol | Access | Value | Description |
|-----|--------|--------|-------|--|
| | | | 0* | separate VBAT and VCC supplies; typical application; autobiasing supplied from V _{BAT} |
| | | | 1 | common VBAT and VCC supplies; applications with permanently active regulator; autobiasing is supplied from V _{CC} |

6.10.5 CAN configuration and status registers

Reset values are indicated by '*'.

Table 18. CAN configuration register (address 041h)

| Bit | Symbol | Access | Value | Description |
|-----|--|--------|-------|--|
| 7:6 | reserved | R | - | always write 00; ignore on read |
| 5 | TXRXLP | R/W | | TXD-to-RXD loopback: |
| | | | 0* | normal TXD and RXD behavior |
| | | | 1 | TXD is forwarded to RXD and CAN bus remains recessive in CAN Active mode |
| 4 | TX2RX2LP ^[1] TJA1445B only | R/W | | TXD2-to-RXD2 loopback: |
| | | | 0* | normal TXD2 and RXD2 behavior |
| | | | 1 | TXD2 is forwarded to RXD2 and CAN bus remains recessive in CAN Active mode |
| 3:2 | reserved | R | - | always write 00; ignore on read |
| 1 | LPL | R/W | | low-power ListenOnly mode enable: |
| | | | 0* | low-power ListenOnly mode disabled |
| | | | 1 | low-power ListenOnly mode enabled |
| 0 | CWC | R/W | | CAN wake-up pattern selection: |
| | | | 0* | ISO 11898-2:2016 wake pattern (dom-rec-dom) |
| | | | 1 | ISO 11898-2:2023 wake pattern (dom-rec-dom-rec) |

[1] GPIO1 configured as second RXD output (RXD2) and GPIO2 configured as second TXD input (TXD2).

Table 19. CAN status register (address 072h)

| Bit | Symbol | Access | Value | Description |
|-----|----------|--------|-------|--|
| 7 | CTS | R | | CAN transceiver status: |
| | | | 0 | CAN transceiver not in Active mode or not ready to transmit |
| | | | 1 | CAN transceiver in Active mode and ready to transmit |
| 6:4 | reserved | R | - | ignore on read |
| 3 | CBSS | R | | CAN bus silence status: |
| | | | 0 | CAN bus activity detected |
| | | | 1 | no CAN bus activity detected for longer than $t_{to(silence)}$ |

Table 19. CAN status register (address 072h)...continued

| Bit | Symbol | Access | Value | Description |
|-----|----------------------------------|--------|-------|-------------------------------|
| 2 | BUSDOMS | R | | BUS clamped dominant status: |
| | | | 0 | CAN bus not clamped dominant |
| | | | 1 | CAN bus clamped dominant |
| 1 | TXD2DOMS <i>TJA1445B only</i> | R | | TXD2 clamped dominant status: |
| | | | 0 | TXD2 not clamped dominant |
| | | | 1 | TXD2 clamped dominant |
| 0 | TXDDOMS | R | | TXD clamped dominant status: |
| | | | 0 | TXD not clamped dominant |
| | | | 1 | TXD clamped dominant |

6.10.6 GPIO configuration and status registers: TJA1445B only

Reset values are indicated by '*'.

Table 20. GPIO polarity configuration register (address 045h)

| Bit | Symbol | Access | Value | Description |
|-----|----------|--------|-------|------------------------------------|
| 7:3 | reserved | R | - | always write 00000; ignore on read |
| 2 | GPP3 | R/W | | GPIO3 polarity: |
| | | | 0* | default polarity |
| | | | 1 | inverted polarity |
| 1 | GPP2 | R/W | | GPIO2 polarity: |
| | | | 0* | default polarity |
| | | | 1 | inverted polarity |
| 0 | GPP1 | R/W | | GPIO1 polarity: |
| | | | 0* | default polarity |
| | | | 1 | inverted polarity |

Table 21. GPIO status register (address 074h)

| Bit | Symbol | Access | Value | Description |
|-----|----------|--------|-------|--------------------|
| 7:4 | reserved | R | - | ignore on read |
| 3 | TXENS | R | | TXEN_N pin status: |
| | | | 0 | TXEN_N LOW |
| | | | 1 | TXEN_N HIGH |
| 2 | GPIO3S | R | | GPIO3 pin status: |
| | | | 0 | GPIO3 LOW |
| | | | 1 | GPIO3 HIGH |
| 1 | GPIO2S | R | | GPIO2 pin status: |
| | | | 0 | GPIO2 LOW |

Table 21. GPIO status register (address 074h)...continued

| Bit | Symbol | Access | Value | Description |
|-----|--------|--------|-------|-------------------|
| | | | 1 | GPIO2 HIGH |
| 0 | GPIO1S | R | | GPIO1 pin status: |
| | | | 0 | GPIO1 LOW |
| | | | 1 | GPIO1 HIGH |

Table 22. GPIO1 configuration register (address 042h)

| Bit | Symbol | Access | Value | Description |
|-----|---------|--------|-----------|---|
| 7:5 | GPIO1C | R/W | | GPIO1 pin configuration: |
| | | | 000 | input: floating output: push-pull |
| | | | 001 | input: pull-up output: open-drain high-side driver |
| | | | 010 | input: pull-down output: high-side driver plus weak pull-down |
| | | | 011* | input: repeater output: open-drain low-side driver |
| | | | 100 | input: repeater output: low-side driver plus weak pull-up |
| | | | 101 - 111 | reserved |
| 4:0 | GPIO1FS | R/W | | GPIO1 function select: |
| | | | 0x00* | GPIO1 inactive; repeater function active, independent of GPIO1C |
| | | | 0x01 | input |
| | | | 0x02 | output: LOW when GPP1 = 0; HIGH when GPP1 = 1 |
| | | | 0x03 | TXEN_N input; CAN transmitter disabled when GPIO pin driven HIGH |
| | | | 0x04 | INT_N interrupt output; active-LOW when GPP1 = 0 (default); active-HIGH when GPP1 = 1 |
| | | | 0x05 | reserved |
| | | | 0x06 | GPIO1 configured as second RXD output (RXD2); CAN bus forwarded to both GPIO1 (RXD2) and RXD |
| | | | 0x07 | reserved |
| | | | 0x08 | GPIO1 configured as second RXD output (RXD2); CAN bus forwarded to GPIO1 (RXD2) only; RXD forced HIGH |
| | | | 0x09 | V _{CC} undervoltage status output (UVCCS) ^[1] |
| | | | 0x0A | TXD dominant status output (TXDDOMS) ^[1] |
| | | | 0x0B | TXD2 dominant status output (TXD2DOMS; available when GPIO2 configured as TXD2) ^[1] |
| | | | 0x0C | wake-up pattern detect output ^[1] |
| | | | 0x0D | wake-up frame detect output ^[1] |

Table 22. GPIO1 configuration register (address 042h)...continued

| Bit | Symbol | Access | Value | Description |
|-----|--------|--------|--------------|---|
| | | | 0x0E | CAN bus biasing status output (HIGH, by default, indicates that CAN bus biasing is active) ^[1] |
| | | | 0x0F | WAKE pin rising edge detect output ^[1] |
| | | | 0x10 | WAKE pin falling edge detect output ^[1] |
| | | | 0x11 | CAN Active mode ready-to-transmit status output (CTS) ^[1] |
| | | | 0x12 | CAN ListenOnly mode status output ^[1] |
| | | | 0x13 | rising edge wake-up detection input |
| | | | 0x14 | falling edge wake-up detection input |
| | | | 0x15 | rising or falling edge edge wake-up detection input |
| | | | 0x16 | INH2 output ^[1] |
| | | | 0x17 to 0x1F | reserved |

[1] Active-HIGH when GPP1 = 0; active-LOW when GPP1 = 1

Table 23. GPIO2 configuration register (address 043h)

| Bit | Symbol | Access | Value | Description |
|-----|---------|--------|-----------|---|
| 7:5 | GPIO2C | R/W | | GPIO2 pin configuration: |
| | | | 000 | input: floating output: push-pull |
| | | | 001 | input: pull-up output: open-drain high-side driver |
| | | | 010 | input: pull-down output: high-side driver plus weak pull-down |
| | | | 011* | input: repeater output: open-drain low-side driver |
| | | | 100 | input: repeater output: low-side driver plus weak pull-up |
| | | | 101 - 111 | reserved |
| 4:0 | GPIO2FS | R/W | | GPIO2 function select: |
| | | | 0x00* | GPIO2 inactive; repeater function active, independent of GPIO2C |
| | | | 0x01 | input |
| | | | 0x02 | output: LOW when GPP2 = 0; HIGH when GPP2 = 1 |
| | | | 0x03 | TXEN_N input; CAN transmitter disabled when GPIO pin driven HIGH |
| | | | 0x04 | INT_N interrupt output; active-LOW when GPP2 = 0 (default); active-HIGH when GPP2 = 1 |
| | | | 0x05 | GPIO2 configured as second TXD input (TXD2); TXD and TXD2 (via GPIO2) data fed to the CAN bus |
| | | | 0x06 | reserved |

Table 23. GPIO2 configuration register (address 043h)...continued

| Bit | Symbol | Access | Value | Description |
|-----|--------|--------|--------------|---|
| | | | 0x07 | GPIO2 configured as second TXD input (TXD2); only TXD2 (via GPIO2) data fed to the CAN bus; TXD input ignored |
| | | | 0x08 | reserved |
| | | | 0x09 | V _{CC} undervoltage status output (UVCCS) ^[1] |
| | | | 0x0A | TXD dominant status output (TXDDOMS) ^[1] |
| | | | 0x0B | reserved |
| | | | 0x0C | wake-up pattern detect output ^[1] |
| | | | 0x0D | wake-up frame detect output ^[1] |
| | | | 0x0E | CAN bus biasing status (HIGH, by default, indicates that CAN bus biasing is active) ^[1] |
| | | | 0x0F | WAKE pin rising edge detect output ^[1] |
| | | | 0x10 | WAKE pin falling edge detect output ^[1] |
| | | | 0x11 | CAN Active mode ready-to-transmit status output (CTS) ^[1] |
| | | | 0x12 | CAN ListenOnly mode status ^[1] |
| | | | 0x13 | rising edge edge wake-up detection input |
| | | | 0x14 | falling edge edge wake-up detection input |
| | | | 0x15 | rising or falling edge edge wake-up detection input |
| | | | 0x16 | INH2 output ^[1] |
| | | | 0x17 to 0x1F | reserved |

[1] Active-HIGH when GPP2 = 0; active-LOW when GPP2 = 1

Table 24. GPIO3 configuration register (address 044h)

| Bit | Symbol | Access | Value | Description |
|-----|--------|--------|-----------|--|
| 7:5 | GPIO3C | R/W | | GPIO3 pin configuration: |
| | | | 000 | input: floating output: push-pull |
| | | | 001 | input: pull-up output: open-drain high-side driver |
| | | | 010 | input: pull-down output: high-side driver plus weak pull-down |
| | | | 011* | input: repeater output: open-drain low-side driver |
| | | | 100 | input: repeater output: low-side driver plus weak pull-up |
| | | | 101 - 111 | reserved |

Table 24. GPIO3 configuration register (address 044h)...continued

| Bit | Symbol | Access | Value | Description |
|-----|---------|--------|--------------|--|
| 4:0 | GPIO3FS | R/W | | GPIO3 function select: |
| | | | 0x00* | GPIO3 inactive; repeater function active, independent of GPIO3C |
| | | | 0x01 | input |
| | | | 0x02 | output: LOW when GPP3 = 0; HIGH when GPP3 = 1 |
| | | | 0x03 | TXEN_N input; CAN transmitter disabled when GPIO pin driven HIGH |
| | | | 0x04 | INT_N interrupt output; active-LOW when GPP3 = 0 (default); active-HIGH when GPP3 = 1 |
| | | | 0x05 | reserved |
| | | | 0x06 | reserved |
| | | | 0x07 | reserved |
| | | | 0x08 | reserved |
| | | | 0x09 | V _{CC} undervoltage status output (UVCCS) ^[1] |
| | | | 0x0A | TXD dominant status output (TXDDOMS) ^[1] |
| | | | 0x0B | TXD2 dominant status output (TXD2DOMS; available when GPIO2 configured as TXD2) ^[1] |
| | | | 0x0C | wake-up pattern detect output ^[1] |
| | | | 0x0D | wake-up frame detect output ^[1] |
| | | | 0x0E | CAN bus biasing status (HIGH, by default, indicates that CAN bus biasing is active) ^[1] |
| | | | 0x0F | WAKE pin rising edge detect output ^[1] |
| | | | 0x10 | WAKE pin falling edge detect output ^[1] |
| | | | 0x11 | CAN Active mode ready-to-transmit status output (CTS) ^[1] |
| | | | 0x12 | CAN ListenOnly mode status ^[1] |
| | | | 0x13 | rising edge edge wake-up detection input |
| | | | 0x14 | falling edge edge wake-up detection input |
| | | | 0x15 | rising or falling edge edge wake-up detection input |
| | | | 0x16 | INH2 output ^[1] |
| | | | 0x17 to 0x1F | reserved |

[1] Active-HIGH when GPP3 = 0; active-LOW when GPP3 = 1

6.10.7 Partial networking registers

Reset values are indicated by '*'.

Table 25. Partial networking status register (address 073h)

| Bit | Symbol | Access | Value | Description |
|-----|----------|--------|-------|--|
| 7 | SYNCS | R | | CAN partial networking sync status: |
| | | | 0 | CAN partial networking core not ready to decode frame |
| | | | 1 | CAN partial networking core ready to decode frame |
| 6 | CPNERRS | R | | CAN partial networking error status: |
| | | | 0 | no CAN partial networking error detected; PNFDER = 0 and PNCOK = 1 |
| | | | 1 | CAN partial networking error detected; PNFDER = 1 or PNCOK = 0; wake-up via WUP only |
| 5 | CPNS | R | | CAN partial networking status: |
| | | | 0 | CAN partial networking configuration error detected; PNCOK = 0 |
| | | | 1 | CAN partial networking configuration OK; PNCOK = 1 |
| 4 | LFDS | R | | last frame decode status: |
| | | | 0 | most recent CAN frame not decoded successfully |
| | | | 1 | most recent CAN frame decoded successfully |
| 3:0 | reserved | R | - | ignore on read |

Table 26. Partial networking error count status register (address 075h)

| Bit | Symbol | Access | Value | Description |
|-----|----------|--------|--------|--|
| 7:5 | reserved | R | - | always write 000; ignore on read |
| 4:0 | PNERRCNT | R/W | | CAN partial networking error count status: |
| | | | 00000* | 0 |
| | | | 00001 | 1 |
| | | | 00010 | 2 |
| | | | 00011 | 3 |
| | | | ... | ... |
| | | | 11111 | 31 |

Table 27. Partial networking ID registers 0 to 3 (addresses 020h to 023h)

| Addr. | Bit | Symbol | Access | Value | Description |
|-------|-----|-----------|--------|-------|--|
| 020h | 7:0 | ID7:ID0 | R/W | 00h* | bits ID7 to ID0 of the extended frame format |
| 021h | 7:0 | ID15:ID8 | R/W | 00h* | bits ID15 to ID8 of the extended frame format |
| 022h | 7:2 | ID23:ID18 | R/W | 00h* | bits ID23 to ID18 of the extended frame format bits ID5 to ID0 of the standard frame format |
| | 1:0 | ID17:ID16 | R/W | 00h* | bits ID17 to ID16 of the extended frame format |

Table 27. Partial networking ID registers 0 to 3 (addresses 020h to 023h)....continued

| Addr. | Bit | Symbol | Access | Value | Description |
|-------|-----|-----------|--------|-------|---|
| 023h | 7:5 | reserved | R/W | 00h* | always write 000; ignore on read |
| | 4:0 | ID28:ID24 | R/W | 00h* | bits ID28 to ID24 of the extended frame format bits ID10 to ID6 of the standard frame format |

Table 28. Partial networking ID mask registers 0 to 3 (addresses 024h to 027h)

| Addr. | Bit | Symbol | Access | Value | Description |
|-------|-----|----------|--------|-------|--|
| 024h | 7:0 | M7:M0 | R/W | 00h* | ID mask bits 7 to 0 of extended frame format |
| 025h | 7:0 | M15:M8 | R/W | 00h* | ID mask bits 15 to 8 of extended frame format |
| 026h | 7:2 | M23:M18 | R/W | 00h* | ID mask bits 23 to 18 of extended frame format ID mask bits 5 to 0 of standard frame format |
| | 1:0 | M17:M16 | R/W | 00h* | ID mask bits 17 to 16 of extended frame format |
| 027h | 7:5 | reserved | R/W | 00h* | always write 000; ignore on read |
| | 4:0 | M28:M24 | R/W | 00h* | ID mask bits 28 to 24 of extended frame format ID mask. bits 10 to 6 of standard frame format |

Table 29. Partial networking data mask registers 0 to 7 (addresses 028h to 02Fh)

All data mask bits are set to 1 by default.

| Addr. | Bit | Symbol | Access | Value | Description |
|-------|-----|--------|--------|-------|---------------------------|
| 028h | 7:0 | DM0 | R/W | FFh* | data mask 0 configuration |
| 029h | 7:0 | DM1 | R/W | FFh* | data mask 1 configuration |
| 02Ah | 7:0 | DM2 | R/W | FFh* | data mask 2 configuration |
| 02Bh | 7:0 | DM3 | R/W | FFh* | data mask 3 configuration |
| 02Ch | 7:0 | DM4 | R/W | FFh* | data mask 4 configuration |
| 02Dh | 7:0 | DM5 | R/W | FFh* | data mask 5 configuration |
| 02Eh | 7:0 | DM6 | R/W | FFh* | data mask 6 configuration |
| 02Fh | 7:0 | DM7 | R/W | FFh* | data mask 7 configuration |

Table 30. Partial networking frame control register (address 030h)

| Bit | Symbol | Access | Value | Description |
|-----|----------|--------|-------|--|
| 7 | IDE | R/W | | identifier format: |
| | | | 0* | standard frame format (11-bit) |
| | | | 1 | extended frame format (29-bit) |
| 6 | PNDM | R/W | | partial networking data mask: |
| | | | 0 | data length code and data field are 'don't care' for wake-up |
| | | | 1* | data length code and data field are evaluated at wake-up |
| 5:4 | reserved | R | - | always write 00; ignore on read |

Table 30. Partial networking frame control register (address 030h)...continued

| Bit | Symbol | Access | Value | Description |
|-----|--------|--------|--------------|---|
| 3:0 | DLC | R/W | | number of data bytes expected in a CAN frame (DLC): |
| | | | 0000* | 0 |
| | | | 0001 | 1 |
| | | | 0010 | 2 |
| | | | 0011 | 3 |
| | | | 0100 | 4 |
| | | | 0101 | 5 |
| | | | 0110 | 6 |
| | | | 0111 | 7 |
| | | | 1000 | 8 |
| | | | 1001 to 1111 | 8 |

Table 31. Partial networking data rate and filter configuration register (address 031h)

| Bit | Symbol | Access | Value | Description |
|-----|----------|--------|--------------|--|
| 7:4 | IDFS | R/W | | idle detection filter select: |
| | | | 0000* | bitfilter 0: ignore < 5.0 % of bit time; detect > 17.5 % of bit time |
| | | | 0001 | ISO bitfilter 1: ignore < 5.0 % of bit time; detect > 17.5 % of bit time |
| | | | 0010 | ISO bitfilter 2: ignore < 2.5 % of bit time; detect > 8.75 % of bit time |
| | | | 0011 | bitfilter 3: ignore < 18 ns; detect > 93 ns |
| | | | 0100 | bitfilter 4: ignore < 42 ns; detect > 119 ns |
| | | | 0101 | bitfilter 5: ignore < 67 ns; detect > 145 ns |
| | | | 0110 | bitfilter 6: ignore < 91 ns; detect > 170 ns |
| | | | 0111 to 1111 | reserved |
| 3 | reserved | R | - | always write 0; ignore on read |
| 2:0 | CDR | R/W | | CAN data rate selection: |
| | | | 000 | 50 kbit/s |
| | | | 001 | 100 kbit/s |
| | | | 010 | 125 kbit/s |
| | | | 011 | 250 kbit/s |
| | | | 100* | 500 kbit/s |
| | | | 101 | 667 kbit/s |
| | | | 110 | reserved (PNCORE disabled) |
| | | | 111 | 1 Mbit/s |

Table 32. Partial networking and CAN configuration register (address 032h)

| Bit | Symbol | Access | Value | Description |
|-----|----------|--------|-------|---|
| 7:3 | reserved | R | - | always write 00000; ignore on read |
| 2 | PNECC | R/W | | partial networking error counter control: |
| | | | 0* | CAN FD frames will increment error counter |
| | | | 1 | CAN FD frames will not increment error counter |
| 1 | PNCOK | R/W | | CAN partial networking configuration: |
| | | | 0* | partial networking register configuration invalid (wake-up via standard wake-up pattern only) |
| | | | 1 | partial networking register configuration valid |
| 0 | CPNC | R/W | | CAN selective wake-up enable: |
| | | | 0* | disable CAN selective wake-up |
| | | | 1 | enable CAN selective wake-up |

6.10.8 System reset register

Table 33. System reset register (address FE0h)

| Bit | Symbol | Access | Value | Description |
|-----|--------|--------|-------|-------------------------------|
| 7:0 | SFR | W | | software-forced system reset: |
| | | | 01h | set up system reset |
| | | | 80h | confirm system reset |

6.10.9 Wake-up pulse configuration register

Reset values are indicated by '*'.

Table 34. Wake-up pulse configuration register (address 040h)

| Bit | Symbol | Access | Value | Description |
|-----|----------|--------|-------|--|
| 7:1 | reserved | R | - | always write 00h; ignore on read |
| 0 | WFC | R/W | | wake-up pulse width (t_{wake}) on WAKE pin |
| | | | 0* | short wake-up time |
| | | | 1 | long wake-up time |

6.10.10 Interrupt registers

Reset values are indicated by '*'.

Write 1 to clear (W1C) interrupt status bit after interrupt detected.

Table 35. System interrupt enable register (address 010h)

| Bit | Symbol | Access | Value | Description |
|-----|--------------------|--------|-------|--------------------------------|
| 7 | reserved | R | - | always write 0; ignore on read |
| 6 | CWE ^[1] | R/W | | CAN wake-up interrupt enable: |
| | | | 0* | disable CAN wake-up interrupt |

Table 35. System interrupt enable register (address 010h)...continued

| Bit | Symbol | Access | Value | Description |
|-----|---------------------|--------|-------|---|
| | | | 1 | enable CAN wake-up interrupt |
| 5 | OTE | R/W | | overtemperature shutdown interrupt enable: |
| | | | 0* | disable overtemperature shutdown interrupt |
| | | | 1 | enable overtemperature shutdown interrupt |
| 4 | SPIFE | R/W | | SPI failure interrupt enable: |
| | | | 0* | disable SPI failure interrupt |
| | | | 1 | enable SPI failure interrupt |
| 3 | UVCCE | R/W | | V _{CC} undervoltage interrupt enable: |
| | | | 0 | disable V _{CC} undervoltage interrupt |
| | | | 1* | enable V _{CC} undervoltage interrupt |
| 2 | LUVIOE | R/W | | long V _{IO} undervoltage interrupt enable: |
| | | | 0 | disable long V _{IO} undervoltage interrupt |
| | | | 1* | enable long V _{IO} undervoltage interrupt |
| 1 | WPRE ^[1] | R/W | | WAKE pin rising-edge interrupt enable: |
| | | | 0* | disable WAKE pin rising-edge interrupt |
| | | | 1 | enable WAKE pin rising-edge interrupt |
| 0 | WPFE ^[1] | R/W | | WAKE pin falling-edge interrupt enable: |
| | | | 0* | disable WAKE pin falling-edge interrupt |
| | | | 1 | enable WAKE pin falling-edge interrupt |

[1] This interrupt is also a wake-up source.

Table 36. CAN interrupt enable register (address 011h)

| Bit | Symbol | Access | Value | Description |
|-----|----------------------------------|--------|-------|---|
| 7:4 | reserved | R | - | always write 0000; ignore on read |
| 3 | CBSE | R/W | | CAN bus silence interrupt enable: |
| | | | 0* | disable CAN bus silence interrupt |
| | | | 1 | enable CAN bus silence interrupt |
| 2 | BUSDOME | R/W | | CAN bus dominant interrupt enable: |
| | | | 0* | disable CAN bus dominant interrupt |
| | | | 1 | enable CAN bus dominant interrupt |
| 1 | TXD2DOME <i>TJA1445B only</i> | R/W | | TXD2 dominant timeout interrupt enable: |
| | | | 0* | disable TXD2 dominant timeout interrupt |
| | | | 1 | enable TXD2 dominant timeout interrupt |
| 0 | TXDDOME | R/W | | TXD dominant timeout interrupt enable: |
| | | | 0* | disable TXD dominant timeout interrupt |
| | | | 1 | enable TXD dominant timeout interrupt |

Table 37. GPIO interrupt enable register (address 012h) - TJA1445B only

| Bit | Symbol | Access | Value | Description |
|-----|----------|--------|-------|------------------------------------|
| 7:3 | reserved | R | - | always write 00000; ignore on read |
| 2 | GPIO3E | R/W | | GPIO2 interrupt enable: |
| | | | 0* | disable GPIO2 interrupt |
| | | | 1 | enable GPIO2 interrupt |
| 1 | GPIO2E | R/W | | GPIO2 interrupt enable: |
| | | | 0* | disable GPIO2 interrupt |
| | | | 1 | enable GPIO2 interrupt |
| 0 | GPIO1E | R/W | | GPIO1 interrupt enable: |
| | | | 0* | disable GPIO1 interrupt |
| | | | 1 | enable GPIO1 interrupt |

Table 38. System interrupt status register (address 060h)

| Bit | Symbol | Access | Value | Description |
|-----|-------------------|--------|-------|---|
| 7 | PO ^[1] | R/W1C | | power-on interrupt: |
| | | | 0 | no power-on interrupt detected |
| | | | 1* | power-on interrupt detected |
| 6 | CW | R/W1C | | CAN wake-up interrupt: |
| | | | 0* | no CAN wake-up interrupt detected |
| | | | 1 | CAN wake-up interrupt detected |
| 5 | OT | R/W1C | | overtemperature warning interrupt: |
| | | | 0* | no overtemperature warning interrupt detected |
| | | | 1 | overtemperature warning interrupt detected |
| 4 | SPIF | R/W1C | | SPI failure interrupt: |
| | | | 0* | no SPI failure interrupt detected |
| | | | 1 | SPI failure interrupt detected |
| 3 | UVCC | R/W1C | | V _{CC} undervoltage interrupt: |
| | | | 0* | no V _{CC} undervoltage interrupt detected |
| | | | 1 | V _{CC} undervoltage interrupt detected |
| 2 | LUVIO | R/W1C | | long V _{IO} undervoltage interrupt: |
| | | | 0* | no long V _{IO} undervoltage interrupt detected |
| | | | 1 | long V _{IO} undervoltage interrupt detected |
| 1 | WPR | R/W1C | | WAKE pin rising-edge interrupt: |
| | | | 0* | no WAKE pin rising-edge interrupt detected |
| | | | 1 | WAKE pin rising-edge interrupt detected |
| 0 | WPF | R/W1C | | WAKE pin falling-edge interrupt: |
| | | | 0* | no WAKE pin falling-edge interrupt detected |

Table 38. System interrupt status register (address 060h)...continued

| Bit | Symbol | Access | Value | Description |
|-----|--------|--------|-------|--|
| | | | 1 | WAKE pin falling-edge interrupt detected |

[1] PO interrupt is always enabled.

Table 39. CAN interrupt status register (address 061h)

| Bit | Symbol | Access | Value | Description |
|-----|---------------------|--------|-------|---|
| 7:4 | reserved | R | - | always write 0000; ignore on read |
| 3 | CBS | R/W1C | | CAN bus silence interrupt: |
| | | | 0* | no CAN bus silence interrupt detected |
| | | | 1 | CAN bus silence interrupt detected |
| 2 | BUSDOM | R/W1C | | CAN bus dominant interrupt: |
| | | | 0* | no CAN bus dominant interrupt detected |
| | | | 1 | CAN bus dominant interrupt detected |
| 1 | reserved TJA1445A | R | - | always write 0; ignore on read |
| 1 | TXD2DOM TJA1445B | R/W1C | | TXD2 dominant timeout interrupt: |
| | | | 0* | no TXD2 dominant timeout interrupt detected |
| | | | 1 | TXD2 dominant timeout interrupt detected |
| 0 | TXDDOM | R/W1C | | TXD dominant timeout interrupt: |
| | | | 0* | no TXD dominant timeout interrupt detected |
| | | | 1 | TXD dominant timeout interrupt detected |

Table 40. Partial networking interrupt status register (address 062h)

| Bit | Symbol | Access | Value | Description |
|-----|-----------------------|--------|-------|--|
| 7:3 | reserved | R | - | ignore on read |
| 2 | PNFDER ^[1] | R/W1C | | partial networking frame detection error interrupt: |
| | | | 0* | no partial networking frame detection error interrupt detected |
| | | | 1 | partial networking frame detection error interrupt detected |
| 1:0 | reserved | R | - | ignore on read |

[1] PNFDER interrupt is always enabled.

Table 41. GPIO interrupt status register (address 063h) - TJA1445B only>

| Bit | Symbol | Access | Value | Description |
|-----|----------|--------|-------|-----------------------------|
| 7:3 | reserved | R | - | ignore on read |
| 2 | GPIO3 | R/W1C | | GPIO3 interrupt: |
| | | | 0* | no GPIO3 interrupt detected |
| | | | 1 | GPIO3 interrupt detected |

Table 41. GPIO interrupt status register (address 063h) - TJA1445B only>...continued

| Bit | Symbol | Access | Value | Description |
|-----|--------|--------|-------|-----------------------------|
| 1 | GPIO2 | R/W1C | | GPIO2 interrupt: |
| | | | 0* | no GPIO2 interrupt detected |
| | | | 1 | GPIO2 interrupt detected |
| 0 | GPIO1 | R/W1C | | GPIO1 interrupt: |
| | | | 0* | no GPIO1 interrupt detected |
| | | | 1 | GPIO1 interrupt detected |

6.10.11 Lock control register

Reset values are indicated by '*'.

Table 42. Lock control register (address 050h)

| Bit | Symbol | Access | Value | Description |
|-----|----------|--------|-------|---|
| 7:5 | reserved | R | - | always write 000; ignore on read |
| 4 | LKGPM | R/W | | Lock control: general-purpose memory registers (0xFF0 to 0xFF3): |
| | | | 0* | SPI write access enabled |
| | | | 1 | SPI write access disabled |
| 3 | LKRST | R/W | | Lock control: system reset register (0xFE0): |
| | | | 0 | SPI write access enabled |
| | | | 1* | SPI write access disabled |
| 2 | LKCFG | R/W | | Lock control: System/Wake/CAN configuration registers (0x40 to 0x46): |
| | | | 0* | SPI write access enabled |
| | | | 1 | SPI write access disabled |
| 1 | LKPNC | R/W | | Lock control: partial networking configuration registers (0x020 to 0x032): |
| | | | 0* | SPI write access enabled |
| | | | 1 | SPI write access disabled |
| 0 | LKIE | R/W | | Lock control: interrupt enable registers (0x010, 0x011, 0x012 - TJA1445B only): |
| | | | 0* | SPI write access enabled |
| | | | 1 | SPI write access disabled |

6.10.12 General-purpose memory registers

The TJA1445 allocates 4 bytes of memory for general-purpose registers used to store user information. The general-purpose registers can be accessed via the SPI at address 0xFF0 to 0xFF3. Note that these registers are not cleared during a software reset.

Table 43. General-purpose memory registers 0 to 3 (addresses FF0h to FF3h)

| Addr. | Bit | Symbol | Access | Value | Description |
|-------|-----|-----------|--------|-------|--------------------------|
| FF0h | 7:0 | GPM[7:0] | R/W | 00h* | general-purpose memory 0 |
| FF1h | 7:0 | GPM[15:8] | R/W | 00h* | general-purpose memory 1 |

Table 43. General-purpose memory registers 0 to 3 (addresses FF0h to FF3h)...continued

| Addr. | Bit | Symbol | Access | Value | Description |
|-------|-----|------------|--------|-------|--------------------------|
| FF2h | 7:0 | GPM[23:16] | R/W | 00h* | general-purpose memory 2 |
| FF3h | 7:0 | GPM[31:24] | R/W | 00h* | general-purpose memory 3 |

6.10.13 Device identification register

Table 44. Device identification register (address FFFh)

| Bit | Symbol | Access | Value | Description |
|-----|--------|--------|------------|-------------------------------|
| 7:0 | IDS | R | - | device identification number: |
| | | | 01h | TJA1445A |
| | | | 02h | TJA1445B |
| | | | 03h to FFh | reserved |

7 Limiting values

Table 45. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134); all voltages are referenced to pin GND, unless otherwise specified; positive currents flow into the IC.

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-------------------|---------------------------------------|--|------|------------------------------|------|
| V_x | Voltage on pin x ^[1] | pins VCC, VIO | -0.3 | +6 | V |
| | | | - | +7 ^[2] | V |
| | | pin VBAT | -0.3 | +40 | V |
| | | pin INH | -0.3 | $V_{BAT}+0.3$ ^[3] | V |
| | | pins CANH, CANL, WAKE | -36 | +40 | V |
| | | pins RXD, TXD, SCSN, SCK, SDI, SDO, TXEN_N, GPIOx | -0.3 | $V_{IO}+0.3$ ^[4] | V |
| $I_{O(INH)}$ | output current on pin INH | | -2 | - | mA |
| $V_{(CANH-CANL)}$ | voltage between pin CANH and pin CANL | | -40 | +40 | V |
| V_{trt} | transient voltage | on pins VBAT, WAKE, CANH, CANL; ISODIS = 0 ^[5] | | | |
| | | pulse 1 | -100 | - | V |
| | | pulse 2a | - | +75 | V |
| | | pulse 3a | -150 | - | V |
| | | pulse 3b | - | +100 | V |
| V_{ESD} | electrostatic discharge voltage | IEC 61000-4-2 (150 pF, 330 Ω discharge circuit) ^[6] | | | |
| | | on pins CANH, CANL; on pin VBAT with 100 nF capacitor; on pin WAKE with 33 k Ω resistor | -8 | +8 | kV |
| | | Human Body Model (HBM) | | | |
| | | on any pin ^[7] | -4 | +4 | kV |
| | | on pins CANH, CANL ^[8] | -8 | +8 | kV |
| | | Charged Device Model (CDM) ^[9] | | | |
| | | on any pin | -500 | +500 | V |
| T_{vj} | virtual junction temperature | | -40 | +150 | °C |
| | | | | | |
| T_{stg} | storage temperature | | -55 | +150 | °C |

[1] The device can sustain voltages up to the specified values over the product lifetime, provided applied voltages (including transients) never exceed these values.

[2] The device can withstand voltages between 6 V and 7 V for a total of 20 s over the product lifetime.

[3] Absolute maximum of 40 V.

[4] Subject to the qualifications detailed in Table notes 1 and 2 above for pin VIO, and for VIO-related input pins.

[5] Verified by an external test house according to IEC TS 62228, Section 4.2.4; parameters for standard pulses defined in ISO 7637, part 2.

[6] Verified by an external test house according to IEC TS 62228, Section 4.3.

[7] According to AEC-Q100-002.

[8] Pins stressed to reference group containing all ground and supply pins, emulating the application circuits (Figure 15 and Figure 16). HBM pulse as specified in AEC-Q100-002 used.

[9] According to AEC-Q100-011.

[10] Only valid for TJA1445AT.

[11] In accordance with IEC 60747-1. An alternative definition of virtual junction temperature is: $T_{vj} = T_{amb} + P \times R_{th(j-a)}$, where $R_{th(j-a)}$ is a fixed value used in the calculation of T_{vj} . The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).

[12] T_{stg} in application according to IEC61360-4. For component transport and storage conditions, see instead IEC61760-2.

8 Thermal characteristics

Table 46. Thermal characteristics

Value determined for free convection conditions on a JEDEC 2S2P board.

| Symbol | Parameter | Conditions ^[1] | Typ | Unit |
|----------------|--|---------------------------|-----|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | SO14 | 85 | K/W |
| | | HVSON14 | 71 | K/W |
| | | DHVQFN18 | 69 | K/W |
| $R_{th(j-c)}$ | thermal resistance from junction to case ^[2] | HVSON14 | 34 | K/W |
| | | DHVQFN18 | 29 | K/W |
| Ψ_{j-top} | thermal characterization parameter from junction to top of package | SO14 | 8 | K/W |
| | | HVSON14 | 11 | K/W |
| | | DHVQFN18 | 9 | K/W |

[1] According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board. Board with two inner copper layers (thickness: 35 μ m) and thermal via array under the exposed pad connected to the first inner copper layer (thickness: 70 μ m).

[2] Case temperature refers to the center of the heatsink at the bottom of the package.

9 Static characteristics

Table 47. Static characteristics

$T_{vj} = -40\text{ }^{\circ}\text{C}$ to $+175\text{ }^{\circ}\text{C}$; $V_{CC} = 4.5\text{ V}$ to 5.5 V ; $V_{IO} = 1.71\text{ V}$ to 5.5 V ; $V_{BAT} = 4.75\text{ V}$ to 40 V ; $R_L = 60\text{ }\Omega$ unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.^[1]

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|---------------------------------|---|-----|-----|-----|---------|
| Supply; pin VCC | | | | | | |
| V_{CC} | supply voltage | | 4.5 | - | 5.5 | V |
| V_{uvd} | undervoltage detection voltage | ^[2] | 4 | - | 4.5 | V |
| V_{uvhys} | undervoltage hysteresis voltage | | 50 | - | - | mV |
| I_{CC} | supply current | Normal mode; dominant; $V_{TXD} = 0\text{ V}$ | | | | |
| | | $t < t_{to(dom)TXD}$ | - | 40 | 60 | mA |
| | | short circuit on bus lines; - $3\text{ V} < (V_{CANH} = V_{CANL}) < +40\text{ V}$ | - | - | 125 | mA |
| | | Normal mode, recessive; $V_{TXD} = V_{IO}$ | - | 6 | 9 | mA |
| | | Listen-only mode, LPL = 0 | - | 6 | 9 | mA |
| | | Listen-only mode; LPL = 1; $V_{BATVCC} = 0$; $T_{vj} < 150\text{ }^{\circ}\text{C}$ | - | - | 23 | μ A |
| | | Listen-only mode; LPL = 1; $V_{BATVCC} = 1$; $T_{vj} < 150\text{ }^{\circ}\text{C}$ | - | 90 | 165 | μ A |
| | | Standby or Sleep mode; $T_{vj} < 85\text{ }^{\circ}\text{C}$ | - | - | 2 | μ A |
| | | Standby or Sleep mode; $T_{vj} < 150\text{ }^{\circ}\text{C}$ | - | - | 23 | μ A |

Table 47. Static characteristics...continued

$T_{vj} = -40\text{ }^{\circ}\text{C}$ to $+175\text{ }^{\circ}\text{C}$; $V_{CC} = 4.5\text{ V}$ to 5.5 V ; $V_{IO} = 1.71\text{ V}$ to 5.5 V ; $V_{BAT} = 4.75\text{ V}$ to 40 V ; $R_t = 60\text{ }\Omega$ unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.^[7]

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------------------|---------------------------------|---|--------------------|------|--------------------|------|
| I/O level adapter supply; pin VIO | | | | | | |
| V _{IO} | supply voltage | | 1.71 | - | 5.5 | V |
| V _{uvd} | undervoltage detection voltage | [2] | 1.5 | - | 1.71 | V |
| V _{uvhys} | undervoltage hysteresis voltage | | 33 | - | - | mV |
| I _{IO} | supply current | Normal or Listen-only mode; V _{TXD} = V _{IO} | - | - | 3 | μA |
| | | Standby or Sleep mode;; T _{vj} < 85 °C | - | - | 2 | μA |
| | | Standby or Sleep mode; T _{vj} < 150 °C | - | - | <tb> | μA |
| Supply; pin VBAT | | | | | | |
| V _{BAT} | battery supply voltage | | 4.75 | - | 40 | V |
| | | extended range | 4.25 | - | 40 | V |
| V _{uvd} | undervoltage detection voltage | [2] | 4.25 | - | 4.75 | V |
| I _{BAT} | battery supply current | Normal mode; pin INH left open; V _{BAT} ≤ 28 V | - | - | 400 | μA |
| | | Listen-only mode; pin INH left open; V _{BAT} ≤ 28 V | - | - | 525 | μA |
| | | Sleep or Standby mode; CAN Offline Bias mode; pin INH left open; CWE = 1; CPNC = 1; PNCOK = 1; V _{WAKE} = V _{BAT} ; V _{BAT} ≤ 28 V | | | | |
| | | VBATVCC = 0; T _{vj} < 85 °C | - | - | 450 | μA |
| | | VBATVCC = 0; T _{vj} < 150 °C | - | - | 500 | μA |
| | | VBATVCC = 1; T _{vj} < 85 °C | - | - | 350 | μA |
| | | VBATVCC = 1; T _{vj} < 150 °C | - | - | 375 | μA |
| | | Sleep or Standby mode; CAN Offline mode; pin INH left open; V _{WAKE} = V _{BAT} ; V _{BAT} ≤ 28 V | | | | |
| | | T _{vj} < 85 °C | - | <tb> | 22 | μA |
| | | T _{vj} < 150 °C | - | <tb> | 30 | μA |
| | | V _{BAT} = 32 V; BCCTRL = 0; additional current due to V _{BAT} being increased to 32 V | | <tb> | 0.5 | mA |
| | | V _{BAT} = 40 V; BCCTRL = 0; additional current due to V _{BAT} being increased to 40 V | | <tb> | 1.8 | mA |
| CAN transmit data input; pin TXD | | | | | | |
| V _{IH} | HIGH-level input voltage | | 0.7V _{IO} | - | - | V |
| V _{IL} | LOW-level input voltage | | - | - | 0.3V _{IO} | V |

Table 47. Static characteristics...continued

$T_{vj} = -40\text{ }^{\circ}\text{C}$ to $+175\text{ }^{\circ}\text{C}$; $V_{CC} = 4.5\text{ V}$ to 5.5 V ; $V_{IO} = 1.71\text{ V}$ to 5.5 V ; $V_{BAT} = 4.75\text{ V}$ to 40 V ; $R_i = 60\text{ }\Omega$ unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.^[7]

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|----------------------------------|---|-------------|-----|-------------|---------------|
| $V_{hys(TXD)}$ | hysteresis voltage on pin TXD | | 50 | - | - | mV |
| R_{pu} | pull-up resistance | | 20 | - | 80 | k Ω |
| $I_{IL(off)}$ | Off state input leakage current | Off or Boot mode or $V_{IO} < V_{uvd(VIO)}$; $0\text{ V} < V_{TXD} < V_{IO}$ | -5 | - | +5 | μA |
| C_i | input capacitance | ^[3] | - | - | 10 | pF |
| CAN receive data output; pin RXD | | | | | | |
| I_{OH} | HIGH-level output current | $V_{RXD} = V_{IO} - 0.4\text{ V}$ | -10 | - | -1 | mA |
| I_{OL} | LOW-level output current | $V_{RXD} = 0.4\text{ V}$ | 1 | - | 10 | mA |
| $I_{IL(off)}$ | Off state input leakage current | Off or Boot mode or $V_{IO} < V_{uvd(VIO)}$; $0\text{ V} < V_{RXD} < V_{IO}$ | -5 | - | +5 | μA |
| Inhibit output pin; pin INH | | | | | | |
| ΔV_H | HIGH-level voltage drop | $\Delta V_H = V_{BAT} - V_{INH}$; $I_{INH} = -1\text{ mA}$ | 0 | - | 1 | V |
| | | $\Delta V_H = V_{BAT} - V_{INH}$; $I_{INH} = -2\text{ mA}$ | 0 | - | 2 | V |
| I_L | leakage current | Sleep mode; Off mode | -2 | - | 2 | μA |
| $I_{O(sc)}$ | short-circuit output current | $V_{INH} = 0\text{ V}$ | -15 | - | -2 | mA |
| Serial peripheral interface | | | | | | |
| input pins SDI, SCK and SCSN | | | | | | |
| V_{IH} | HIGH-level input voltage | | $0.7V_{IO}$ | - | - | V |
| V_{IL} | LOW-level input voltage | | - | - | $0.3V_{IO}$ | V |
| V_{hys} | hysteresis voltage | | 50 | - | - | mV |
| R_{pd} | pull-down resistance | on pins SCK and SDI; $V_{SCK} = V_{IL}$; $V_{SDI} = V_{IL}$ | 20 | - | 80 | k Ω |
| R_{pu} | pull-up resistance | on pins SCK and SDI; $V_{SCK} = V_{IH}$; $V_{SDI} = V_{IH}$ | 20 | - | 80 | k Ω |
| | | on pin SCSN | 20 | - | 80 | k Ω |
| $I_{IL(off)}$ | Off state input leakage current | pins SDI and SCK; Off or Boot mode or $V_{IO} < V_{uvd(VIO)}$; $0\text{ V} < V_{SDI} < V_{IO}$; $0\text{ V} < V_{SCK} < V_{IO}$ | -5 | - | +5 | μA |
| C_i | input capacitance | | - | - | 10 | pF |
| output pin SDO | | | | | | |
| I_{OH} | HIGH-level output current | $V_{SDO} = V_{IO} - 0.4\text{ V}$ | -10 | - | -1 | mA |
| I_{OL} | LOW-level output current | $V_{SDO} = 0.4\text{ V}$ | 1 | - | 10 | mA |
| $I_{OL(off)}$ | Off state output leakage current | $V_{SCSN} = V_{IO}$ or Off or Boot mode or $V_{IO} < V_{uvd(VIO)}$; $0\text{ V} < V_{SDO} < V_{IO}$ | -5 | - | +5 | μA |
| General purpose I/Os; pins GPIOx (TJA1445B only) | | | | | | |
| I_{OH} | HIGH-level output current | $V_{GPIOx} = V_{IO} - 0.4\text{ V}$; depending on GPIO configuration | -10 | - | -1 | mA |

Table 47. Static characteristics...continued

$T_{vj} = -40\text{ }^{\circ}\text{C}$ to $+175\text{ }^{\circ}\text{C}$; $V_{CC} = 4.5\text{ V}$ to 5.5 V ; $V_{IO} = 1.71\text{ V}$ to 5.5 V ; $V_{BAT} = 4.75\text{ V}$ to 40 V ; $R_L = 60\text{ }\Omega$ unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.^[7]

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|----------------------------------|--|-------------|-----|-------------|---------------|
| I_{OL} | LOW-level output current | $V_{GPIOx} = 0.4\text{ V}$; depending on GPIO configuration | 1 | - | 10 | mA |
| V_{IH} | HIGH-level input voltage | depending on GPIO configuration | $0.7V_{IO}$ | - | - | V |
| V_{IL} | LOW-level input voltage | depending on GPIO configuration | - | - | $0.3V_{IO}$ | V |
| V_{hys} | hysteresis voltage | depending on GPIO configuration | 50 | - | - | mV |
| R_{pu} | pull-up resistance | depending on GPIO configuration | 20 | - | 80 | k Ω |
| R_{pd} | pull-down resistance | depending on GPIO configuration | 20 | - | 80 | k Ω |
| $I_{OL(off)}$ | Off state output leakage current | high-Z or $V_{IO} < V_{lvd}(V_{IO})$; $0\text{ V} < V_{GPIOx} < V_{IO}$ | -5 | - | 5 | μA |
| C_i | input capacitance | ^[3] | - | - | 10 | pF |
| Transmitter enable/disable input; pin TXEN_N (TJA1445B only) | | | | | | |
| V_{IH} | HIGH-level input voltage | | $0.7V_{IO}$ | - | - | V |
| V_{IL} | LOW-level input voltage | | - | - | $0.3V_{IO}$ | V |
| V_{hys} | hysteresis voltage | | 50 | - | - | mV |
| R_{pu} | pull-up resistance | | 20 | - | 80 | k Ω |
| C_i | input capacitance | ^[3] | - | - | 10 | pF |
| Local wake-up input; pin WAKE | | | | | | |
| R_{pu} | pull-up resistance | $V_{WAKE} > V_{th(wake)(max)}$ for $t > t_{wake(max)}$ | 100 | - | 400 | k Ω |
| R_{pd} | pull-down resistance | $V_{WAKE} < V_{th(wake)(min)}$ for $t > t_{wake(max)}$ | 100 | - | 400 | k Ω |
| $V_{th(wake)}$ | wake-up threshold voltage | Sleep or Standby mode | 1.8 | - | 2.6 | V |
| V_{hys} | hysteresis voltage | | 90 | - | - | mV |
| Bus lines; pins CANH and CANL | | | | | | |
| $V_{O(dom)}$ | dominant output voltage | CAN Active mode; $V_{TXD} = 0\text{ V}$; $t < t_{to(dom)TXD}$; $V_{CC} \geq 4.75\text{ V}$ | | | | |
| | | pin CANH; $R_L = 50\text{ }\Omega$ to $65\text{ }\Omega$ | 2.75 | 3.5 | 4.5 | V |
| | | pin CANL; $R_L = 50\text{ }\Omega$ to $65\text{ }\Omega$ | 0.5 | 1.5 | 2.25 | V |
| V_{TXsym} | transmitter voltage symmetry | $V_{TXsym} = V_{CANH} + V_{CANL}$; $C_{SPLIT} = 4.7\text{ nF}$; $f_{TXD} = 250\text{ kHz}$, 1 MHz or 2.5 MHz ^[3] ^[4] | $0.9V_{CC}$ | - | $1.1V_{CC}$ | V |
| $V_{cm(step)}$ | common mode voltage step | ^[3] ^[4] ^[5] | -150 | - | +150 | mV |
| $V_{cm(p-p)}$ | peak-to-peak common mode voltage | ^[3] ^[4] ^[5] | -300 | - | +300 | mV |
| $V_{O(dif)}$ | differential output voltage | CAN Active mode; dominant; Normal mode; $V_{CC} \geq 4.75$; $V_{TXD} = 0\text{ V}$; $t < t_{to(dom)TXD}$ ^[4] | | | | |
| | | $R_L = 50\text{ }\Omega$ to $65\text{ }\Omega$ | 1.5 | - | 3 | V |

Table 47. Static characteristics...continued

$T_{vj} = -40\text{ }^{\circ}\text{C}$ to $+175\text{ }^{\circ}\text{C}$; $V_{CC} = 4.5\text{ V}$ to 5.5 V ; $V_{IO} = 1.71\text{ V}$ to 5.5 V ; $V_{BAT} = 4.75\text{ V}$ to 40 V ; $R_i = 60\text{ }\Omega$ unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.^[7]

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|--|---|------|-----|------|---------------|
| | | $R_L = 45\text{ }\Omega$ to $70\text{ }\Omega$ | 1.4 | - | 3.3 | V |
| | | $R_L = 2240\text{ }\Omega$ ^[3] | 1.5 | - | 5 | V |
| | | CAN Active mode; recessive; no load | | | | |
| | | recessive; CAN Active, CAN Listen-only or CAN Offline Bias mode; $V_{TXD} = V_{IO}$ | -50 | - | +50 | mV |
| | | CAN Offline mode; no load | -0.2 | - | +0.2 | V |
| $V_{O(rec)}$ | recessive output voltage | CAN Active, CAN Listen-only or CAN Offline Bias mode; $V_{TXD} = V_{IO}$; $VBATVCC = 1$ or $VBATVCC = 0$ and $V_{BAT} \geq 5.5\text{ V}$; no load | 2 | 2.5 | 3 | V |
| | | CAN Offline mode; no load | -0.1 | 0 | +0.1 | V |
| $V_{th(RX)dif}$ | differential receiver threshold voltage | $-12\text{ V} \leq V_{CANH} \leq +12\text{ V}$; $-12\text{ V} \leq V_{CANL} \leq +12\text{ V}$ | | | | |
| | | CAN Active, CAN Listen-only or CAN Offline Bias mode | 0.5 | - | 0.9 | V |
| | | CAN Offline mode | 0.4 | - | 1.1 | V |
| $V_{rec(RX)}$ | receiver recessive voltage | $-12\text{ V} \leq V_{CANH} \leq +12\text{ V}$; $-12\text{ V} \leq V_{CANL} \leq +12\text{ V}$ | | | | |
| | | CAN Active, CAN Listen-only or CAN Offline Bias mode | -4 | - | +0.5 | V |
| | | CAN Offline mode | -4 | - | +0.4 | V |
| $V_{dom(RX)}$ | receiver dominant voltage | $-12\text{ V} \leq V_{CANH} \leq +12\text{ V}$; $-12\text{ V} \leq V_{CANL} \leq +12\text{ V}$ | | | | |
| | | CAN Active, CAN Listen-only or CAN Offline Bias mode | 0.9 | - | 9 | V |
| | | CAN Offline mode | 1.1 | - | 9 | V |
| $V_{hys(RX)dif}$ | differential receiver hysteresis voltage | $-12\text{ V} \leq V_{CANH} \leq +12\text{ V}$; $-12\text{ V} \leq V_{CANL} \leq +12\text{ V}$; CAN Active, CAN Listen-only or CAN Offline Bias mode; no load | 50 | - | - | mV |
| $I_{O(sc)}$ | short-circuit output current | $-15\text{ V} \leq V_{CANH} \leq +40\text{ V}$; $-15\text{ V} \leq V_{CANL} \leq +40\text{ V}$ | - | - | 115 | mA |
| $I_{O(sc)rec}$ | recessive short-circuit output current | $-27\text{ V} \leq V_{CANH} \leq +32\text{ V}$; $-27\text{ V} \leq V_{CANL} \leq +32\text{ V}$; Normal or Listen-only mode; $V_{TXD} = V_{IO}$ | -3 | - | +3 | mA |
| I_L | leakage current | $V_{CC} = V_{IO} = V_{BAT} = 0\text{ V}$ or pins shorted to GND via $47\text{ k}\Omega$; $V_{CANH} = V_{CANL} = 5\text{ V}$; | -10 | - | +10 | μA |
| R_i | input resistance | $-2\text{ V} \leq V_{CANL} \leq +7\text{ V}$; $-2\text{ V} \leq V_{CANH} \leq +7\text{ V}$ | 16 | 32 | 50 | k Ω |
| ΔR_i | input resistance deviation | $0\text{ V} \leq V_{CANL} \leq +5\text{ V}$; $0\text{ V} \leq V_{CANH} \leq +5\text{ V}$ | -3 | - | +3 | % |
| $R_{i(dif)}$ | differential input resistance | $-2\text{ V} \leq V_{CANL} \leq +7\text{ V}$; $-2\text{ V} \leq V_{CANH} \leq +7\text{ V}$ | 32 | 64 | 100 | k Ω |
| C_i | input capacitance | ^[3] | - | - | 20 | pF |

Table 47. Static characteristics...continued

T_{vj} = -40 °C to +175°C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 1.71 V to 5.5 V; V_{BAT} = 4.75 V to 40 V; R_I = 60 Ω unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.^[7]

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------|---------------------------------------|------------|-----|-----|-----|------|
| $C_{l(dif)}$ | differential input capacitance | [3] | - | - | 10 | pF |
| Temperature detection | | | | | | |
| $T_{j(sd)}$ | shutdown junction temperature | [3] | 180 | - | 200 | °C |
| $T_{j(sd)rel}$ | release shutdown junction temperature | [3] | 175 | - | 195 | °C |

- [1] All parameters are guaranteed over the junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage ranges.
- [2] Undervoltage is detected between min and max values. Undervoltage is guaranteed to be detected below min value and guaranteed not to be detected above max value.
- [3] Not tested in production; guaranteed by design.
- [4] The test circuit used to measure the bus output voltage symmetry and the common-mode voltages (which includes C_{SPLIT}) is shown in [Figure 18](#).
- [5] See [Figure 11](#).

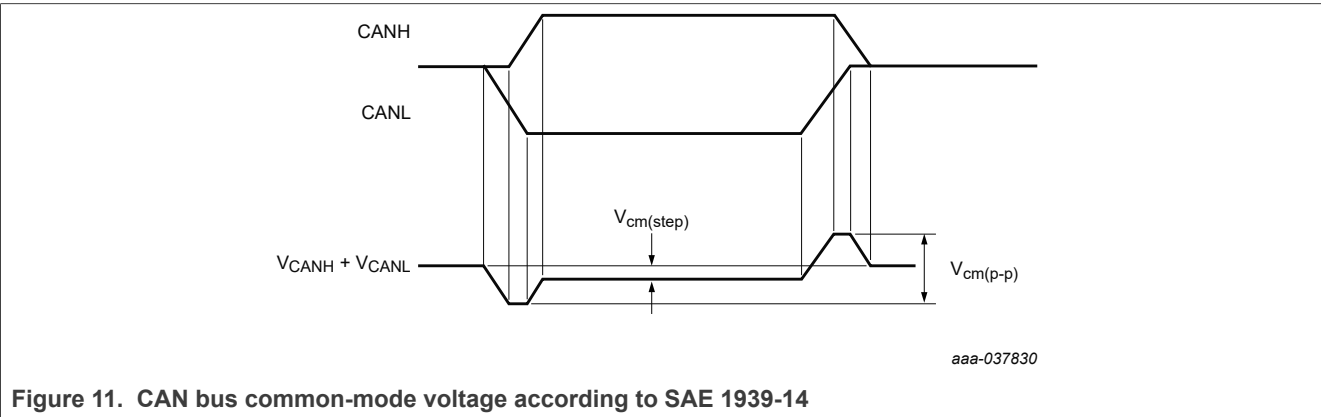


Figure 11. CAN bus common-mode voltage according to SAE 1939-14

10 Dynamic characteristics

Table 48. Dynamic characteristics

$T_{vj} = -40\text{ }^{\circ}\text{C}$ to $+175\text{ }^{\circ}\text{C}$; $V_{CC} = 4.5\text{ V}$ to 5.5 V ; $V_{IO} = 1.71\text{ V}$ to 5.5 V ; $V_{BAT} = 4.5\text{ V}$ to 40 V ; $R_L = 60\text{ }\Omega$ unless specified otherwise; all voltages are defined with respect to ground.^[1]

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|--------------------------------------|---|-----|-----|-------|------|
| CAN timing characteristics; $t_{bit(TXD)} \geq 200$ ns; see Figure 12 , Figure 13 and Figure 17 | | | | | | |
| $t_{d(TXD-busdom)}$ | delay time from TXD to bus dominant | Normal mode | - | - | 102.5 | ns |
| $t_{d(TXD-busrec)}$ | delay time from TXD to bus recessive | Normal mode | - | - | 102.5 | ns |
| $t_{d(busdom-RXD)}$ | delay time from bus dominant to RXD | Normal or Listen-Only mode | - | - | 131 | ns |
| $t_{d(busrec-RXD)}$ | delay time from bus recessive to RXD | Normal or Listen-Only mode | - | - | 131 | ns |
| $t_{d(TXDL-RXDL)}$ | delay time from TXD LOW to RXD LOW | Normal mode | - | - | 210 | ns |
| $t_{d(TXDH-RXDH)}$ | delay time from TXD HIGH to RXD HIGH | Normal mode | - | - | 210 | ns |
| CAN FD timing characteristics according to ISO 11898-2:2016; see Figure 13 and Figure 17 | | | | | | |
| $t_{bit(bus)}^{[2]}$ | transmitted recessive bit width | 2 Mbit/s ($t_{bit(TXD)} = 500$ ns) | 435 | - | 530 | ns |
| | | 5 Mbit/s ($t_{bit(TXD)} = 200$ ns) | 155 | - | 210 | ns |
| Δt_{rec} | receiver timing symmetry | 2 Mbit/s | -65 | - | +40 | ns |
| | | 5 Mbit/s | -45 | - | +15 | ns |
| $t_{bit(RXD)}^{[3]}$ | bit time on pin RXD | 2 Mbit/s ($t_{bit(TXD)} = 500$ ns) | 400 | - | 550 | ns |
| | | 5 Mbit/s ($t_{bit(TXD)} = 200$ ns) | 120 | - | 220 | ns |
| Dominant time-out times | | | | | | |
| $t_{to(dom)TXD}$ | TXD dominant time-out time | $V_{TXD} = 0$ V; Normal mode ^{[4][5]} | 0.8 | - | 4 | ms |
| $t_{to(dom)bus}$ | bus dominant time-out time | $V_{O(dif)} > 0.9$ V; Normal or Listen-Only mode ^{[4][5]} | 0.8 | - | 4 | ms |
| Bus wake-up times; pins CANH and CANL; see Figure 6 and Figure 7 | | | | | | |
| $t_{wake(busdom)}$ | bus dominant wake-up time | CAN Offline mode ^{[4][6]} | 0.5 | - | 1.45 | µs |
| $t_{wake(busrec)}$ | bus recessive wake-up time | CAN Offline mode ^{[4][6]} | 0.5 | - | 1.45 | µs |
| $t_{to(wake)bus}$ | bus wake-up time-out time | CAN Offline mode ^{[4][5]} | 0.8 | - | 9 | ms |
| $t_{d(busact-bias)}$ | bus bias reaction time | CAN Offline mode | - | - | 250 | µs |
| $t_{to(silence)}$ | bus silence time-out time | timer reset and restarted when bus changes from dominant to recessive or vice versa | 0.6 | - | 1.2 | s |
| Serial peripheral interface timing; pins SCSN, SCK, SDI and SDO; see Figure 14 | | | | | | |
| $t_{cy(clk)}$ | clock cycle time | Normal, Listen-Only, Standby or Sleep mode | 250 | - | - | ns |
| $t_{SPILEAD}$ | SPI enable lead time | Normal, Listen-Only, Standby or Sleep mode | 50 | - | - | ns |

Table 48. Dynamic characteristics...continued

$T_{vj} = -40\text{ }^{\circ}\text{C}$ to $+175\text{ }^{\circ}\text{C}$; $V_{CC} = 4.5\text{ V}$ to 5.5 V ; $V_{IO} = 1.71\text{ V}$ to 5.5 V ; $V_{BAT} = 4.5\text{ V}$ to 40 V ; $R_L = 60\text{ }\Omega$ unless specified otherwise; all voltages are defined with respect to ground.^[1]

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|-------------------------------------|---|-----|-----|------|------|
| t_{SPILAG} | SPI enable lag time | Normal, Listen-Only, Standby or Sleep mode | 50 | - | - | ns |
| $t_{clk(H)}$ | clock HIGH time | Normal, Listen-Only, Standby or Sleep mode | 100 | - | - | ns |
| $t_{clk(L)}$ | clock LOW time | Normal, Listen-Only, Standby or Sleep mode | 100 | - | - | ns |
| $t_{su(D)}$ | data input set-up time | Normal, Listen-Only, Standby or Sleep mode | 50 | - | - | ns |
| $t_{h(D)}$ | data input hold time | Normal, Listen-Only, Standby or Sleep mode | 50 | - | - | ns |
| $t_{v(Q)}$ | data output valid time | $C_L = 30\text{ pF}$; Normal, Listen-Only, Standby or Sleep mode; pin SDO | - | - | 50 | ns |
| $d(\text{SDI-SDO})$ | SDI to SDO delay time | $C_L = 30\text{ pF}$; Normal, Listen-Only, Standby or Sleep mode; SPI address bits and read-only bit; pin SDO | - | - | 50 | ns |
| $t_{WH(S)}$ | chip select pulse width HIGH | Normal, Listen-Only, Standby or Sleep mode | 250 | - | - | ns |
| $t_{d(\text{SCKL-SCSN})}$ | delay time from SCK LOW to SCSN LOW | Normal, Listen-Only, Standby or Sleep mode; pin SCSN | 50 | - | - | ns |
| $t_{to(\text{SPI})}$ ^[7] | SPI time-out time | | 1.6 | - | 2.4 | ms |
| CAN partial networking | | | | | | |
| $N_{\text{bit}(\text{idle})}$ | number of idle bits | before a SOF is accepted; ^[4] CWE = 1; CPNC = 1; PNCOK = 1 | 6 | - | 10 | - |
| $t_{\text{fltr}(\text{bit})\text{dom}}$ | dominant bit filter time | arbitration data rate \leq 500 kbit/s; CWE = 1; CPNC = 1; PNCOK = 1; PNECC = 1; IDFS = 0x0 ^[4] ^[8] | 5 | - | 17.5 | % |
| | | data phase bit rate less than or equal to four times the arbitration bit rate or 2 Mbit/s, whichever is lower; CWE = 1; CPNC = 1; PNCOK = 1; PNECC = 1; IDFS = 0x1 ^[4] ^[8] | 5 | - | 17.5 | % |
| | | data phase bit rate less than or equal to ten times the arbitration bit rate or 5 Mbit/s, whichever is lower; CWE = 1; CPNC = 1; PNCOK = 1; PNECC = 1; IDFS = 0x2 ^[4] | 2.5 | - | 8.75 | % |
| | | CWE = 1; CPNC = 1; PNCOK = 1; PNECC = 1; IDFS = 0x3 ^[4] | 18 | - | 93 | ns |

Table 48. Dynamic characteristics...continued

$T_{vj} = -40\text{ }^{\circ}\text{C}$ to $+175\text{ }^{\circ}\text{C}$; $V_{CC} = 4.5\text{ V}$ to 5.5 V ; $V_{IO} = 1.71\text{ V}$ to 5.5 V ; $V_{BAT} = 4.5\text{ V}$ to 40 V ; $R_L = 60\text{ }\Omega$ unless specified otherwise; all voltages are defined with respect to ground.^[1]

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|-----------------------------|--|------|-----|------|------|
| | | CWE = 1; CPNC = 1; PNCOK = 1; PNECC = 1; IDFS = 0x4 ^[4] | 42 | - | 119 | ns |
| | | CWE = 1; CPNC = 1; PNCOK = 1; PNECC = 1; IDFS = 0x5 ^[4] | 67 | - | 145 | ns |
| | | CWE = 1, CPNC = 1, PNCOK = 1, PNECC = 1; IDFS = 0x6 ^[4] | 91 | - | 170 | ns |
| Interrupt time-up time; pin RXD; GPIOx (when configured as an interrupt output; TJA1445B only) | | | | | | |
| t _{to(int)} | interrupt time-out time | | 0.9 | - | 1.1 | ms |
| General purpose I/Os; pins GPIOx (TJA1445B only) | | | | | | |
| t _{fltr} | filter time | pin configured as input except when TXD2 option is selected for GPIO2 ^[9] | 1 | - | 10 | μs |
| t _{w(min)} | minimum pulse width | pin configured as output except when RXD2 option is selected for GPIO1 | 3 | - | - | μs |
| Transmitter enable/disable input; pin TXEN_N (TJA1445B only) | | | | | | |
| t _{fltr} | filter time | ^[9] | 1 | - | 5 | μs |
| Mode transitions; see Section 6.2 , Figure 6 and Figure 7 | | | | | | |
| t _{t(moch)} | mode change transition time | ^[4] | - | - | 50 | μs |
| t _{startup} | start-up time | ^[4] | - | - | 1 | ms |
| t _{startup(RXD)} | RXD start-up time | after local or remote wake-up detected ^[4] ^[10] | 0 | - | 20 | μs |
| t _{startup(INH)} | INH start-up time | after local or remote wake-up detected; transition from Sleep to Standby ^[4] ^[11] | 0 | - | 40 | μs |
| t _{t(snm)} | SNM transition time | bus dominant time for Start-to- Normal mode boot | 11 | - | 16 | ms |
| t _{to(MCU)} | MCU time-out time | LUVIOSEL = 0 | 940 | - | 1300 | ms |
| | | LUVIOSEL = 1 | 1880 | - | 2600 | ms |
| Local wake-up input; pin WAKE, see Section 6.2.2 and Table 34 | | | | | | |
| t _{wake} | wake-up time | in response to a falling or rising edge on pin WAKE; Standby or Sleep mode ^[12] | | | | |
| | | short wake-up time: WFC = 0 | 20 | - | 50 | μs |
| | | long wake-up time: WFC = 1 | 12 | - | 18 | ms |
| Undervoltage detection; see Section 6.2 and Figure 5 | | | | | | |
| t _{det(uv)} | undervoltage detection time | ≥ 100 mV input overdrive | | | | |

Table 48. Dynamic characteristics...continued

$T_{vj} = -40\text{ }^{\circ}\text{C}$ to $+175\text{ }^{\circ}\text{C}$; $V_{CC} = 4.5\text{ V}$ to 5.5 V ; $V_{IO} = 1.71\text{ V}$ to 5.5 V ; $V_{BAT} = 4.5\text{ V}$ to 40 V ; $R_L = 60\text{ }\Omega$ unless specified otherwise; all voltages are defined with respect to ground.^[1]

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------------------|----------------------------------|---|-----|-----|------|---------------|
| | | on pin VBAT ^[4] | - | - | 30 | μs |
| | | on pin VCC ^[4] | - | - | 30 | μs |
| | | on pin VIO ^[4] | - | - | 30 | μs |
| $t_{\text{det(}uv\text{)long}}$ | long undervoltage detection time | on pin VIO; LUVIOSEL = 0; $t_{\text{det(}uv\text{)long1}}$ ^[4] ^[13] | 100 | - | 160 | ms |
| | | on pin VIO; LUVIOSEL = 1; $t_{\text{det(}uv\text{)long2}}$ ^[4] ^[13] | 850 | - | 1150 | ms |
| $t_{\text{rec(}uv\text{)}}$ | undervoltage recovery time | $\geq 100\text{ mV}$ input overdrive | | | | |
| | | on pin VBAT ^[4] | - | - | 50 | μs |
| | | on pin VCC ^[4] | - | - | 50 | μs |
| | | on pin VIO ^[4] | - | - | 50 | μs |

[1] All parameters are guaranteed over the junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage ranges.

[2] $t_{\text{bit(bus)}} = \Delta t_{\text{bit(bus)}} + t_{\text{bit(TXD)}}$.

[3] $t_{\text{bit(RXD)}} = \Delta t_{\text{bit(RXD)}} + t_{\text{bit(TXD)}}$.

[4] Not tested in production; guaranteed by design

[5] Time-out occurs between the min and max values. Time-out is guaranteed not to occur below the min value; time-out is guaranteed to occur above the max value.

[6] A dominant/recessive phase shorter than the min value is guaranteed not to be seen as a dominant/recessive bit; a dominant/recessive phase longer than the max value is guaranteed to be seen as a dominant/recessive bit.

[7] See [Section 6.10.1](#).

[8] Up to 2 Mbit/s data speed.

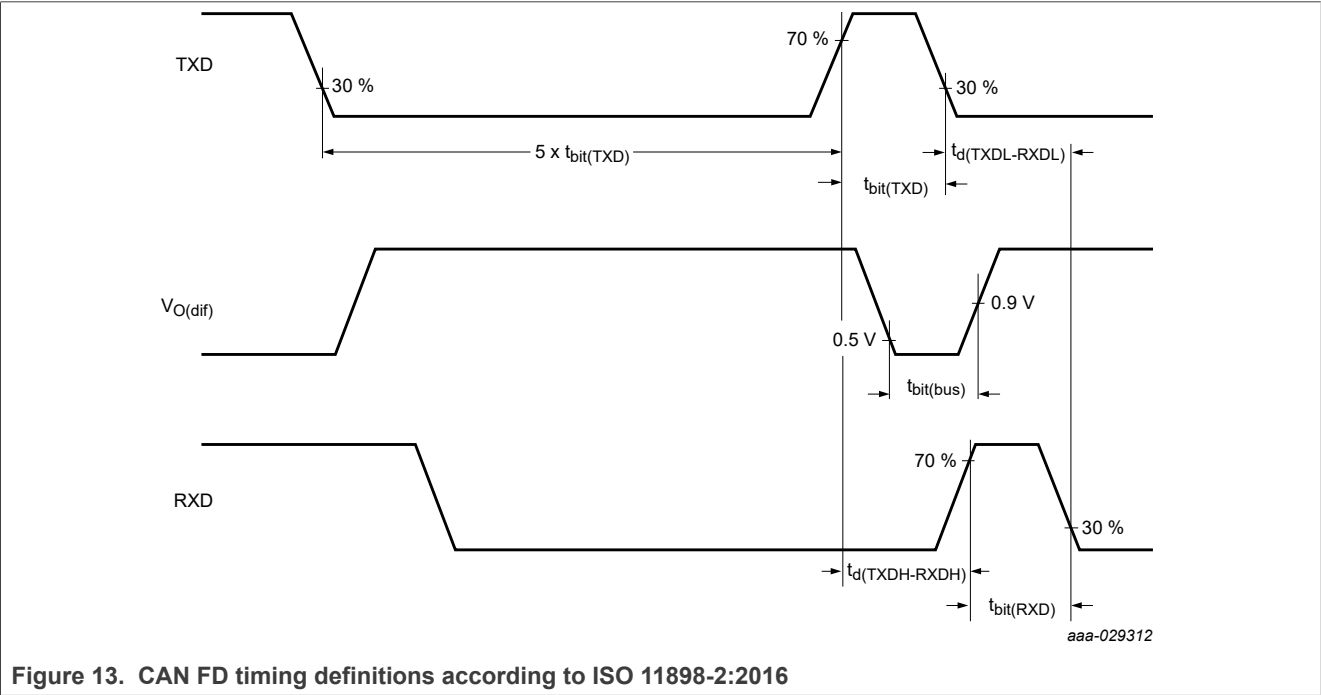
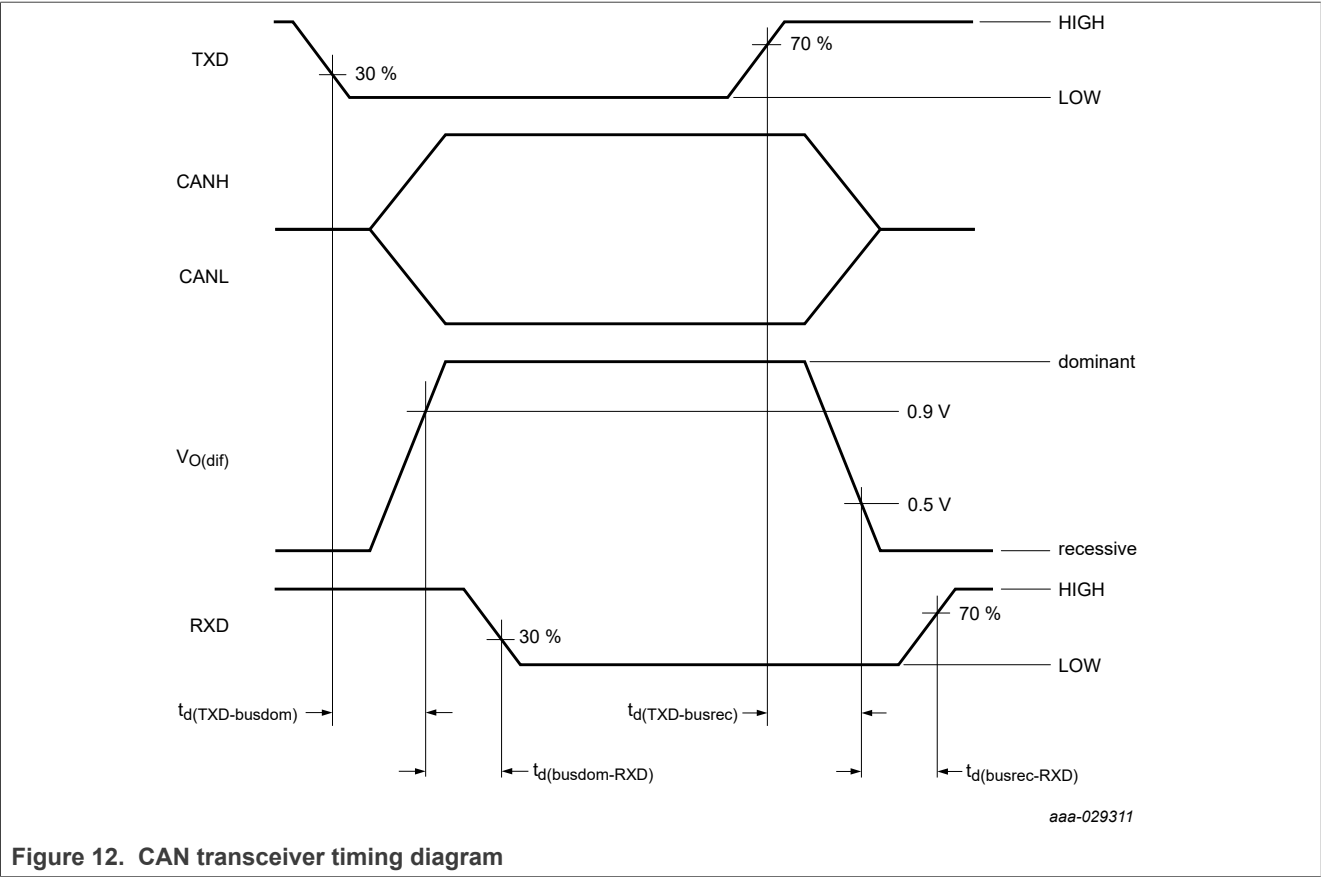
[9] Pulses shorter than the min value are guaranteed to be filtered out; pulses longer than the max value are guaranteed to be processed.

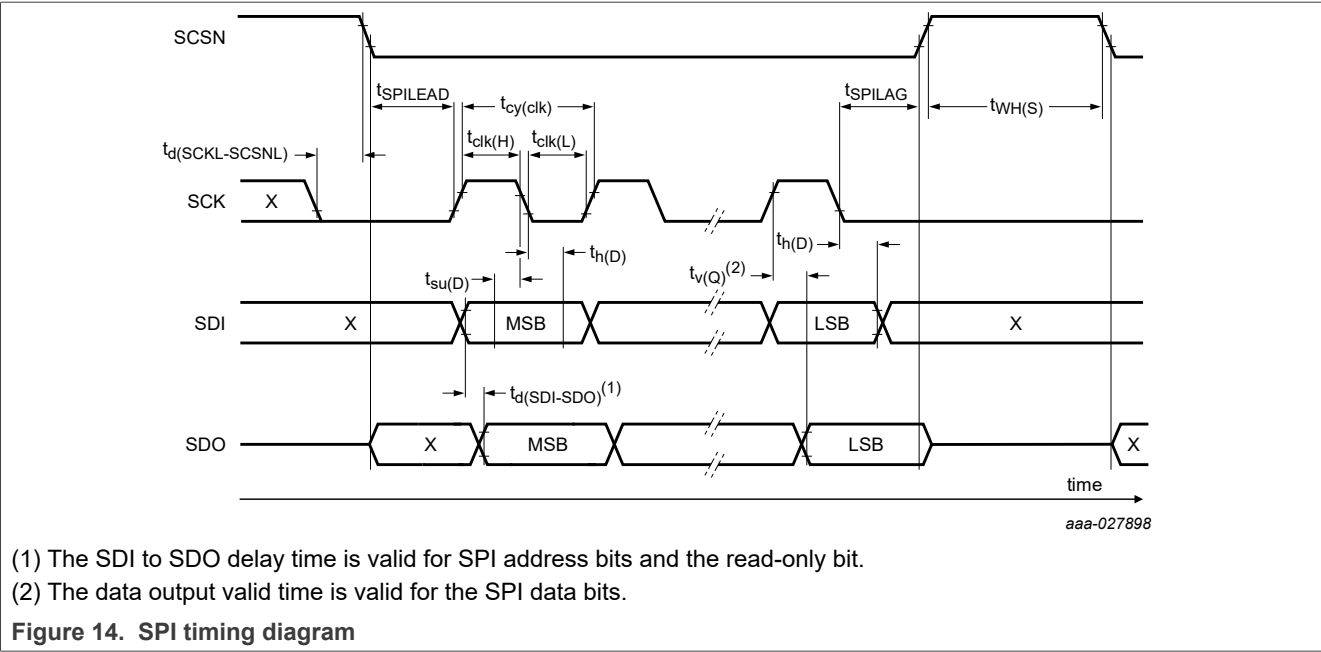
[10] When a wake-up is detected, RXD start-up time is between the min and max values. RXD cannot be relied on below the min value; RXD can be relied on above the max value; see [Figure 6](#) and [Figure 7](#).

[11] INH switches HIGH between the min and max values after a wake-up had been detected. INH is guaranteed to be floating below the min value and guaranteed to be HIGH above the max value; see [Figure 6](#) and [Figure 7](#).

[12] The device is guaranteed to wake up above the max. value and guaranteed not to wake up below the min. value.

[13] An undervoltage longer than the max value is guaranteed to force a transition to Sleep mode; an undervoltage shorter than the min value is guaranteed not to force a transition to Sleep mode.

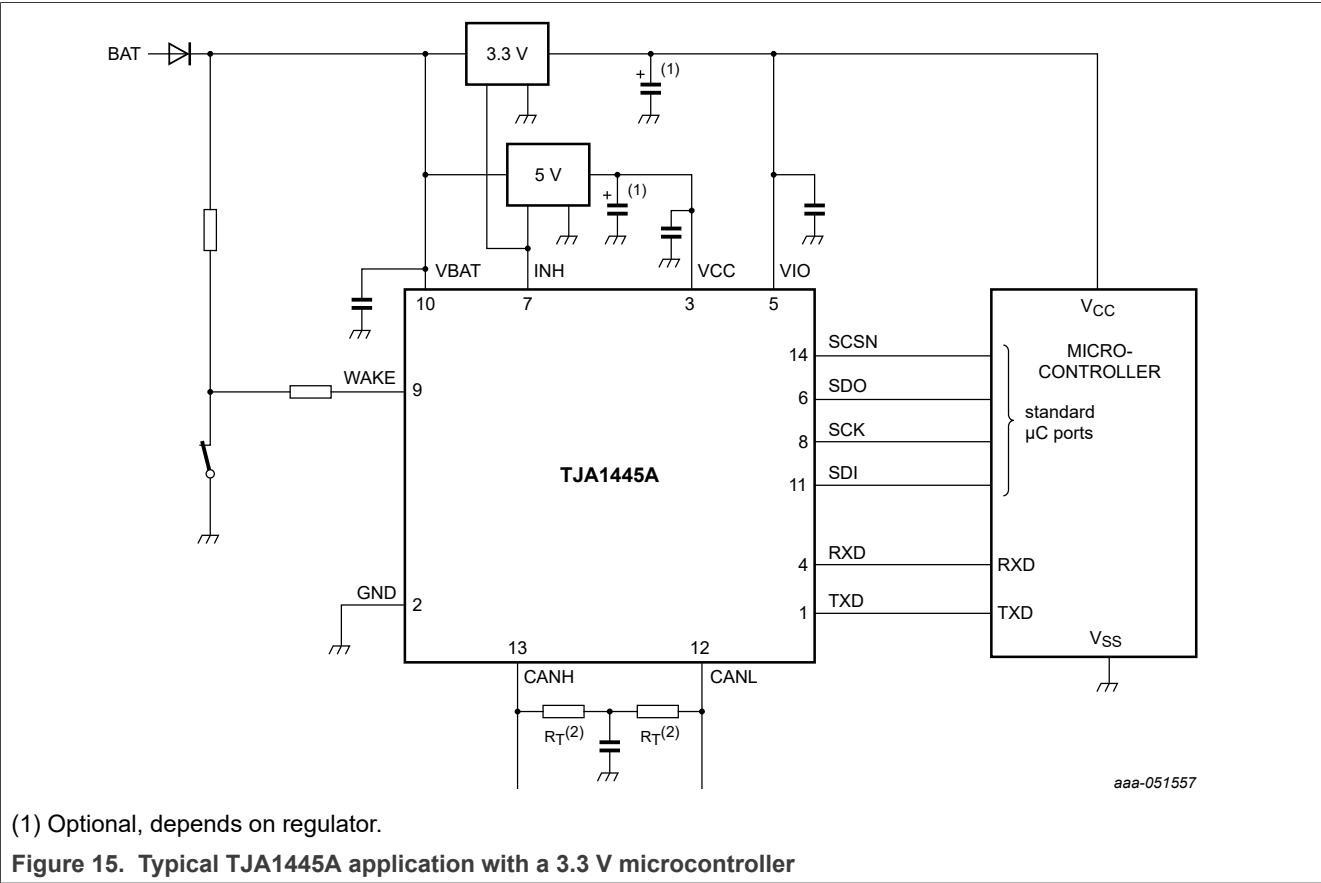


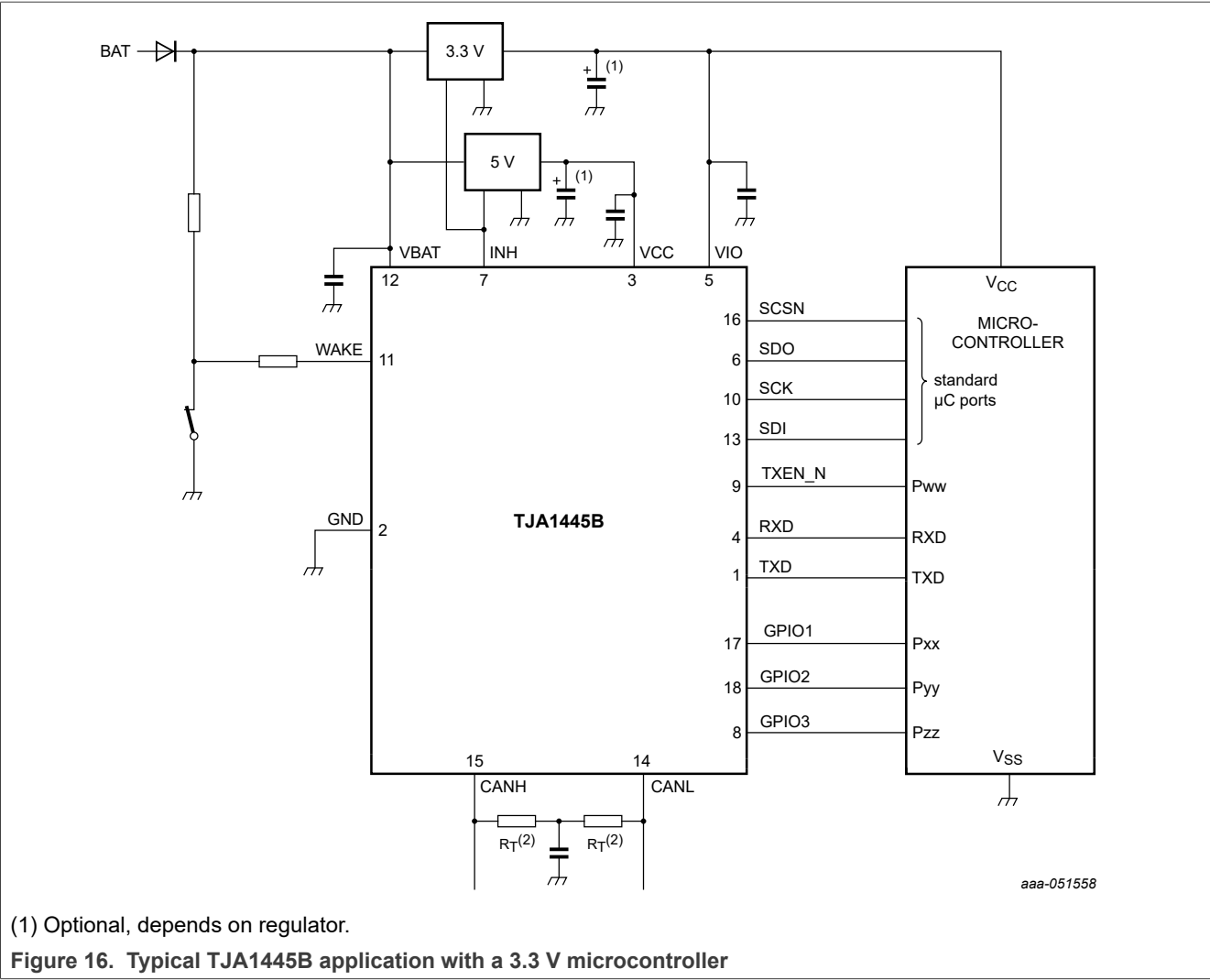


11 Application information

The minimum external circuitry needed with the TJA1445 is shown in [Figure 15](#) and [Figure 16](#). See the application hints ([Section 11.2](#)) for further information about external components and PCB layout requirements.

11.1 Application diagram

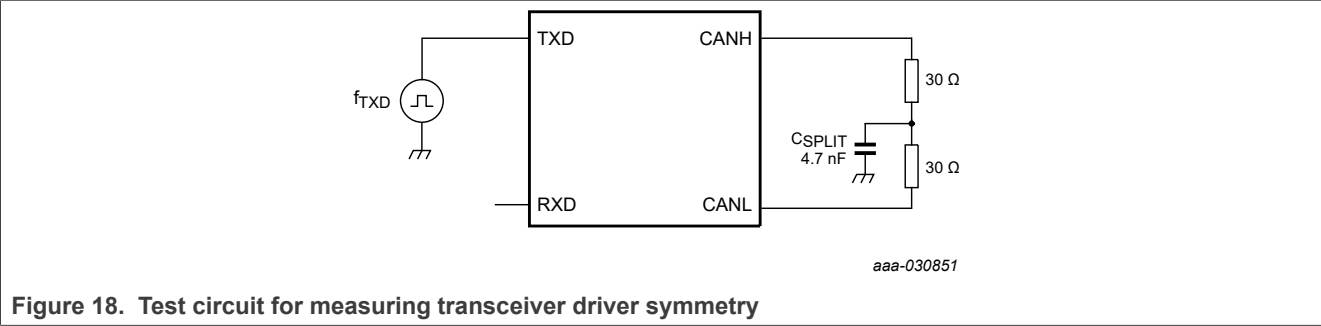
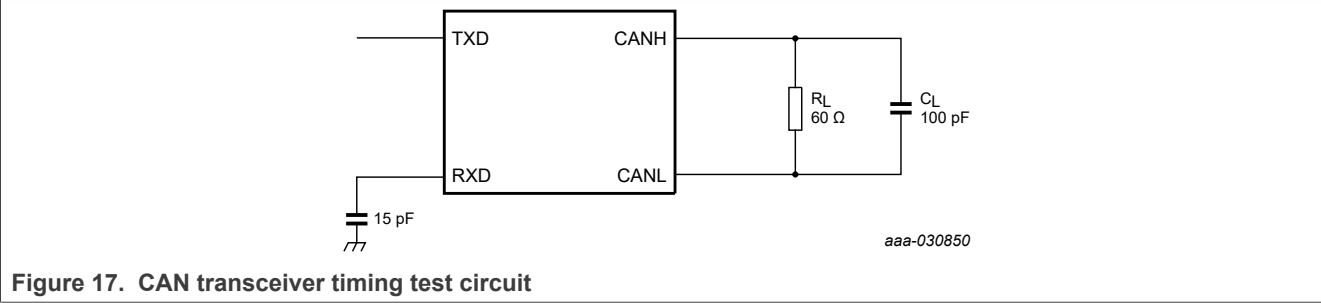




11.2 Application hints

Further information on the application of the TJA1445 can be found in NXP application hints AHxxxx 'TxxxxApplication Hints', available on request from NXP Semiconductors.

12 Test information



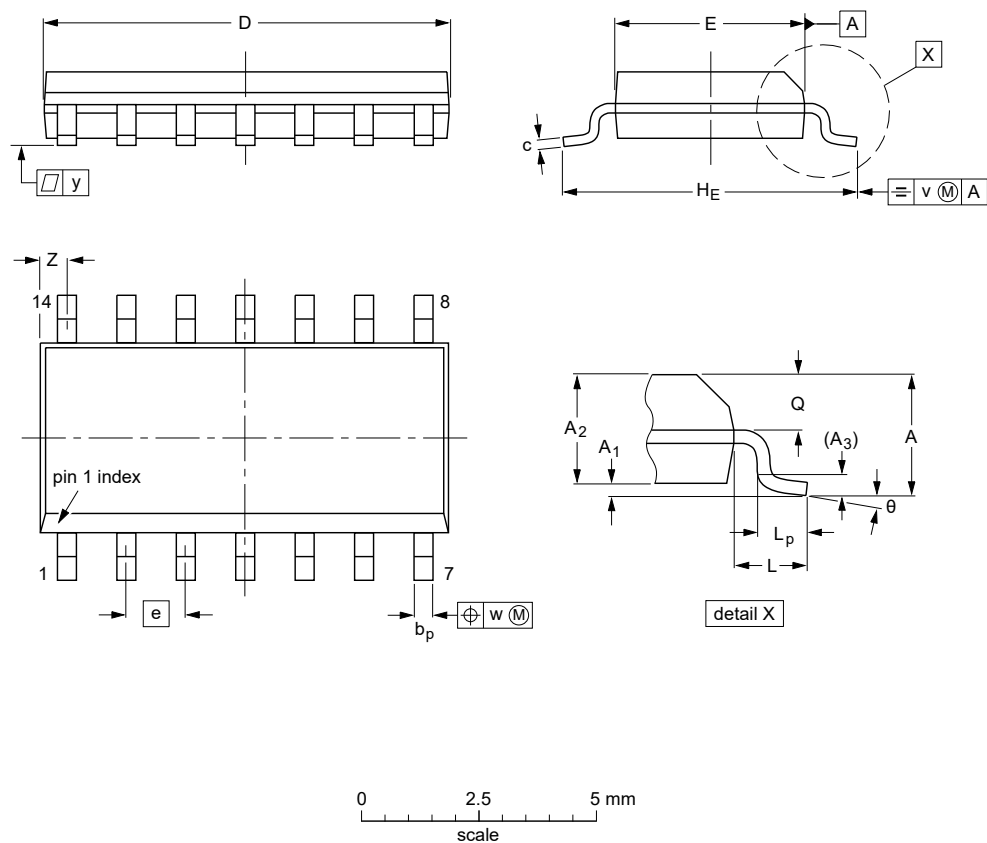
12.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q100 Rev-H - Failure mechanism based stress test qualification for integrated circuits, and is suitable for use in automotive applications.

13 Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A _{max.} | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|--------|-------------------|----------------|----------------|----------------|----------------|------------------|------------------|------------------|------|----------------|-------|----------------|----------------|------|------|-------|------------------|----------|
| mm | 1.75 | 0.25 0.10 | 1.45 1.25 | 0.25 | 0.49 0.36 | 0.25 0.19 | 8.75 8.55 | 4.0 3.8 | 1.27 | 6.2 5.8 | 1.05 | 1.0 0.4 | 0.7 0.6 | 0.25 | 0.25 | 0.1 | 0.7 0.3 | 8° 0° |
| inches | 0.069 | 0.010 0.004 | 0.057 0.049 | 0.01 | 0.019 0.014 | 0.0100 0.0075 | 0.35 0.34 | 0.16 0.15 | 0.05 | 0.244 0.228 | 0.041 | 0.039 0.016 | 0.028 0.024 | 0.01 | 0.01 | 0.004 | 0.028 0.012 | |

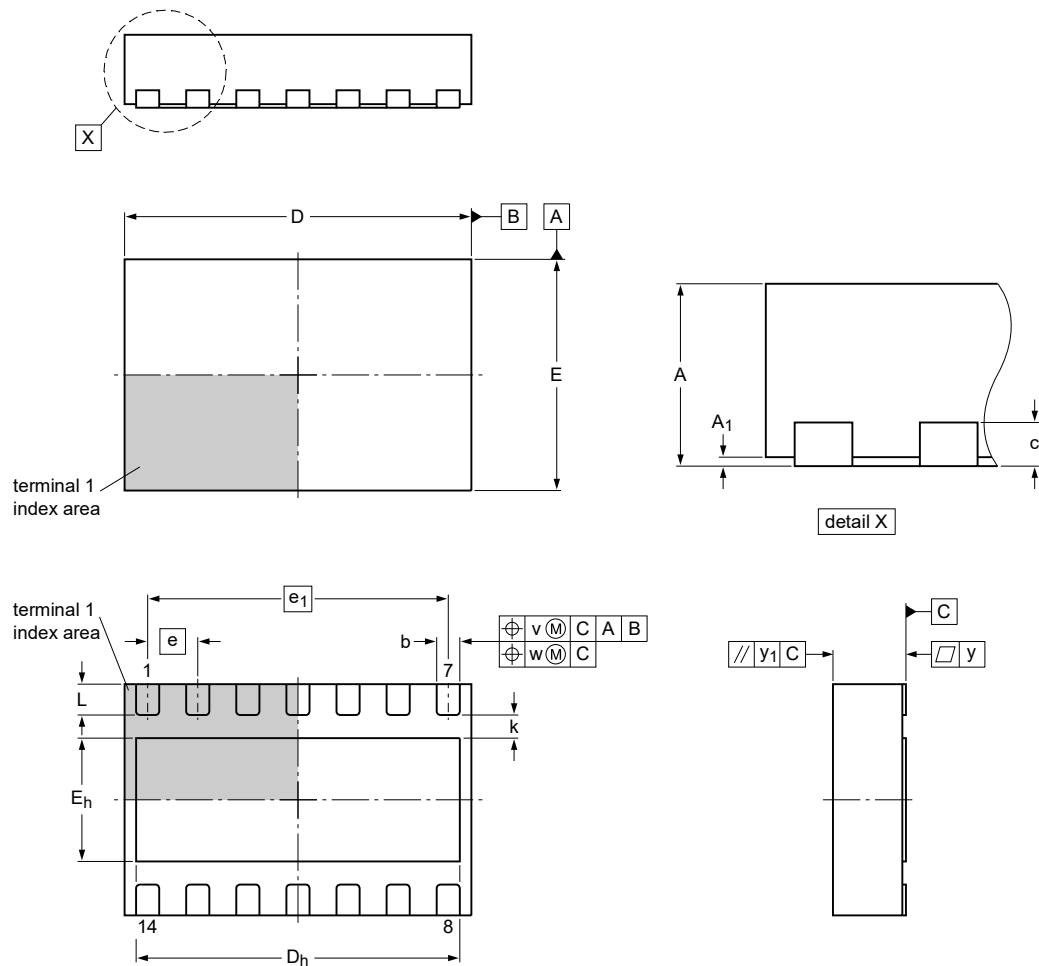
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|--------------------|------------|--------|-------|--|------------------------|----------------------|
| | IEC | JEDEC | JEITA | | | |
| SOT108-1 | 076E06 | MS-012 | | | | 99-12-27 03-02-19 |

Figure 19. Package outline SOT108-1 (SO14)

HVSON14: plastic, thermal enhanced very thin small outline package; no leads;
14 terminals; body 3 x 4.5 x 0.85 mm
SOT1086-2

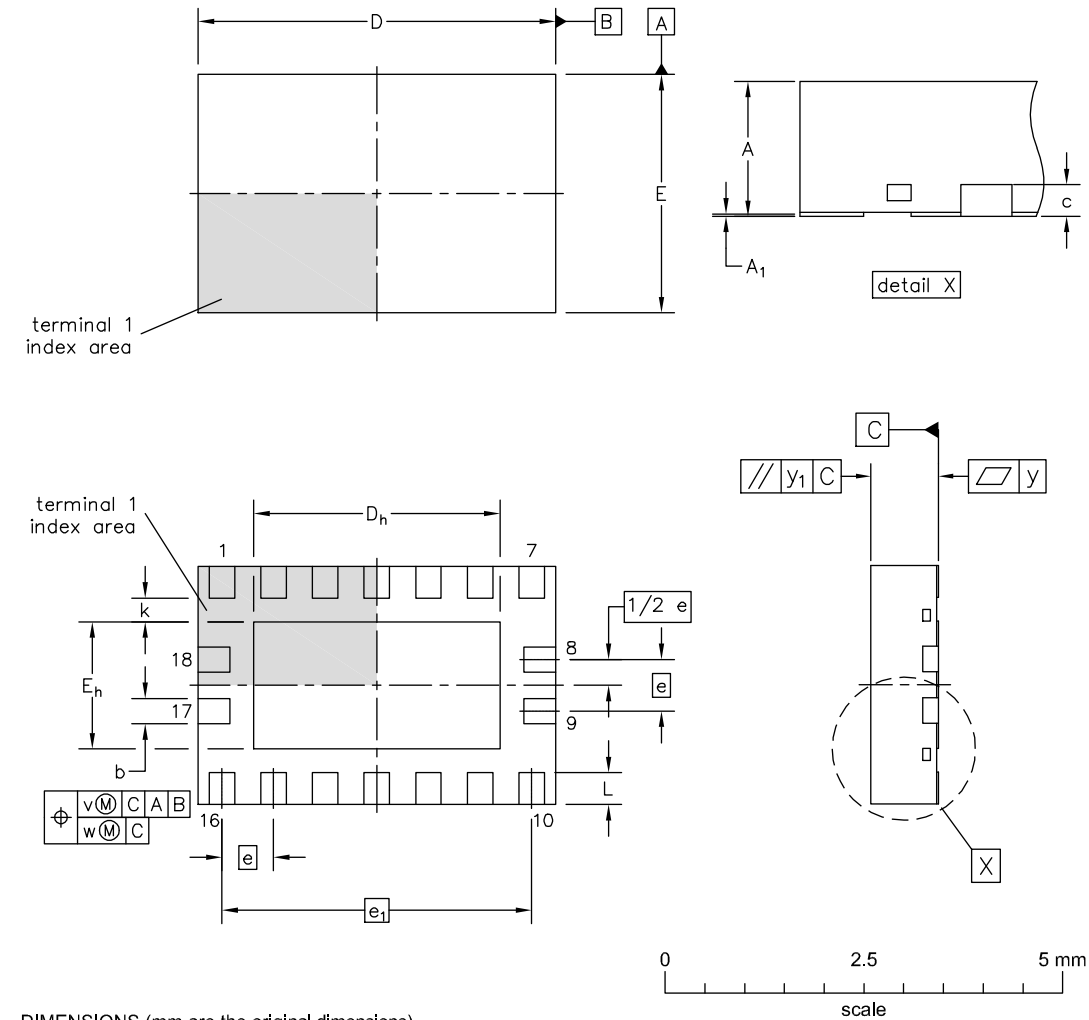


| Unit | A | A ₁ | b | c | D | D _h | E | E _h | e | e ₁ | k | L | v | w | y | y ₁ |
|--------|------|----------------|------|-----|-----|----------------|-----|----------------|------|----------------|------|------|-----|------|------|----------------|
| max | 1.00 | 0.05 | 0.35 | | 4.6 | 4.25 | 3.1 | 1.65 | | 0.35 | 0.45 | | | | | |
| mm nom | 0.85 | 0.03 | 0.32 | 0.2 | 4.5 | 4.20 | 3.0 | 1.60 | 0.65 | 3.9 | 0.30 | 0.40 | 0.1 | 0.05 | 0.05 | 0.1 |
| min | 0.80 | 0.00 | 0.29 | | 4.4 | 4.15 | 2.9 | 1.55 | | 0.25 | 0.35 | | | | | |

| | | | | | | | | | |
|-----------------|-----|------------|-------|--|--|---------------------|--|------------|----------------------|
| | | References | | | | European projection | | Issue date | |
| Outline version | IEC | JEDEC | JEITA | | | | | | |
| SOT1086-2 | --- | MO-229 | --- | | | | | | 10-07-14 10-07-15 |

Figure 20. Package outline SOT1086-2 (HVSON14)

DHVQFN18: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 18 terminals; body 3.0 x 4.5 x 0.85 mm SOT2163-1



DIMENSIONS (mm are the original dimensions)

| Unit ⁽¹⁾ | A | A ₁ | b | c | D | D _h | E | E _h | e | e ₁ | k | L | v | w | y | y ₁ |
|---------------------|------|----------------|------|------|------|----------------|------|----------------|------|----------------|------|------|------|------|------|----------------|
| max | 1.00 | 0.05 | 0.35 | 0.20 | 4.60 | 3.15 | 3.10 | 1.65 | 0.65 | 3.90 | 0.35 | 0.45 | 0.10 | 0.05 | 0.05 | 0.10 |
| nom | 0.85 | 0.03 | 0.32 | | 4.50 | 3.10 | 3.00 | 1.60 | | | 0.30 | 0.40 | | | | |
| min | 0.80 | 0.00 | 0.29 | | 4.40 | 3.05 | 2.90 | 1.55 | | | 0.25 | 0.35 | | | | |

Note
1. Plastic or metal protusions of 0.075 mm maximum per side are not included.

| | | | | | |
|--|------------------------|--------------------------------|----------------|-------------------|--|
| © NXP B.V. ALL RIGHTS RESERVED | | | | DATE: 06 DEC 2022 | |
| MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE | STANDARD: NON JEDEC | DRAWING NUMBER: 98ASA01851D | REVISION: O | | |

Figure 21. Package outline SOT2163-1 (DHVQFN18)

14 Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

15 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leadless SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leadless packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 22](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 49](#) and [Table 50](#)

Table 49. SnPb eutectic process (from J-STD-020D)

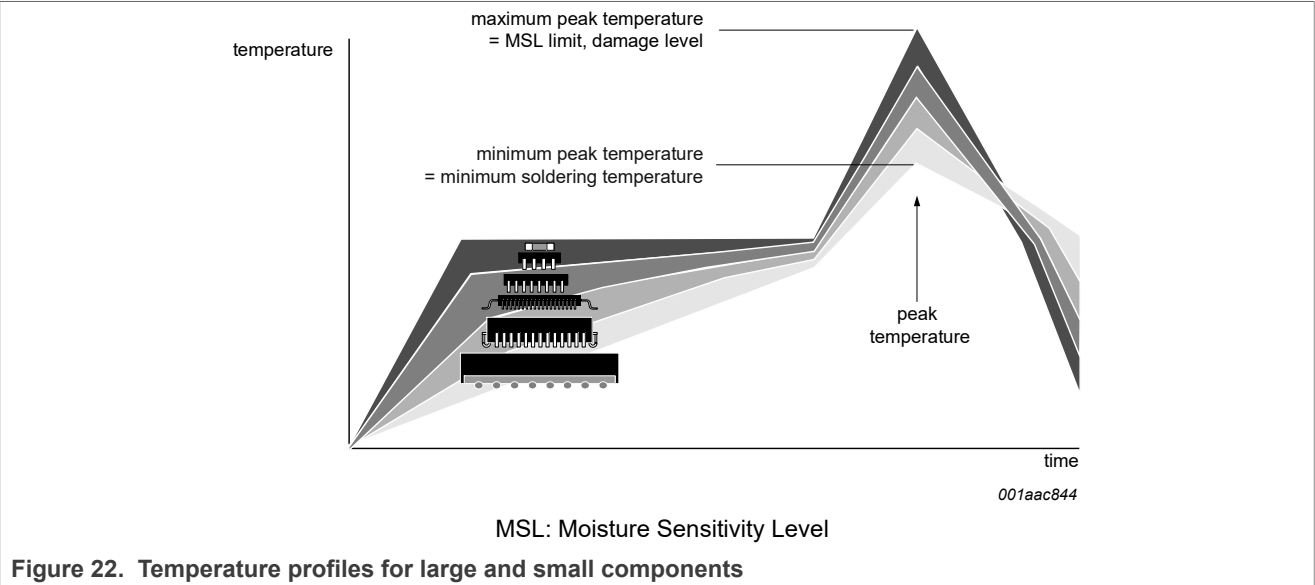
| Package thickness (mm) | Package reflow temperature (°C) | |
|------------------------|---------------------------------|-------|
| | Volume (mm³) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

Table 50. Lead-free process (from J-STD-020D)

| Package thickness (mm) | Package reflow temperature (°C) | | |
|------------------------|---------------------------------|-------------|--------|
| | Volume (mm³) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 22](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

16 Appendix: ISO 11898-2:2016 parameter cross-reference lists

Table 51. ISO 11898-2:2016 to NXP data sheet parameter conversion

| ISO 11898-2:2016 | | NXP data sheet | |
|---|--|---------------------------|---|
| Parameter | Notation | Symbol | Parameter |
| HS-PMA dominant output characteristics | | | |
| Single ended voltage on CAN_H | V _{CAN_H} | V _{O(dom)} | dominant output voltage |
| Single ended voltage on CAN_L | V _{CAN_L} | | |
| Differential voltage on normal bus load | V _{Diff} | V _{O(dif)} | differential output voltage |
| Differential voltage on effective resistance during arbitration | | | |
| Optional: Differential voltage on extended bus load range | | | |
| HS-PMA driver symmetry | | | |
| Driver symmetry | V _{SYM} | V _{TXsym} | transmitter voltage symmetry |
| Maximum HS-PMA driver output current | | | |
| Absolute current on CAN_H | I _{CAN_H} | I _{O(sc)} | short-circuit output current |
| Absolute current on CAN_L | I _{CAN_L} | | |
| HS-PMA recessive output characteristics, bus biasing active/inactive | | | |
| Single ended output voltage on CAN_H | V _{CAN_H} | V _{O(rec)} | recessive output voltage |
| Single ended output voltage on CAN_L | V _{CAN_L} | | |
| Differential output voltage | V _{Diff} | V _{O(dif)} | differential output voltage |
| Optional HS-PMA transmit dominant time-out | | | |
| Transmit dominant time-out, long | t _{dom} | t _{to(dom)} TXD | TXD dominant time-out time |
| Transmit dominant time-out, short | | | |
| HS-PMA static receiver input characteristics, bus biasing active/inactive | | | |
| Recessive state differential input voltage range | V _{Diff} | V _{th(RX)dif} | differential receiver threshold voltage |
| Dominant state differential input voltage range | | V _{rec(RX)} | receiver recessive voltage |
| | | V _{dom(RX)} | receiver dominant voltage |
| HS-PMA receiver input resistance (matching) | | | |
| Differential internal resistance | R _{Diff} | R _{i(dif)} | differential input resistance |
| Single ended internal resistance | R _{CAN_H} R _{CAN_L} | R _i | input resistance |
| Matching of internal resistance | MR | ΔR _i | input resistance deviation |
| HS-PMA implementation loop delay requirement | | | |
| Loop delay | t _{Loop} | t _{d(TXDH-RXDH)} | delay time from TXD HIGH to RXD HIGH |
| | | t _{d(TXDL-RXDL)} | delay time from TXD LOW to RXD LOW |

Table 51. ISO 11898-2:2016 to NXP data sheet parameter conversion...continued

| ISO 11898-2:2016 | | NXP data sheet | |
|---|--|--|---------------------------------------|
| Parameter | Notation | Symbol | Parameter |
| Optional HS-PMA implementation data signal timing requirements for use with bit rates above 1 Mbit/s up to 2 Mbit/s and above 2 Mbit/s up to 5 Mbit/s | | | |
| Transmitted recessive bit width @ 2 Mbit/s / @ 5 Mbit/s, intended | t _{Bit(Bus)} | t _{bit(bus)} | transmitted recessive bit width |
| Received recessive bit width @ 2 Mbit/s / @ 5 Mbit/s | t _{Bit(RXD)} | t _{bit(RXD)} | bit time on pin RXD |
| Receiver timing symmetry @ 2 Mbit/s / @ 5 Mbit/s | Δt _{Rec} | Δt _{rec} | receiver timing symmetry |
| HS-PMA maximum ratings of V _{CAN_H} , V _{CAN_L} and V _{Diff} | | | |
| Maximum rating V _{Diff} | V _{Diff} | V _(CANH-CANL) | voltage between pin CANH and pin CANL |
| General maximum rating V _{CAN_H} and V _{CAN_L} | V _{CAN_H} | V _x | voltage on pin x |
| Optional: Extended maximum rating V _{CAN_H} and V _{CAN_L} | V _{CAN_L} | | |
| HS-PMA maximum leakage currents on CAN_H and CAN_L, unpowered | | | |
| Leakage current on CAN_H, CAN_L | I _{CAN_H} I _{CAN_L} | I _L | leakage current |
| HS-PMA bus biasing control timings | | | |
| CAN activity filter time, long | t _{Filter} | t _{wake(busdom)} ^[1] | bus dominant wake-up time |
| CAN activity filter time, short | | t _{wake(busrec)} | bus recessive wake-up time |
| Wake-up time-out, short | t _{Wake} | t _{to(wake)bus} | bus wake-up time-out time |
| Wake-up time-out, long | | | |

[1] $t_{\text{filtr(wake)bus}}$ - bus wake-up filter time, in devices with basic wake-up functionality

17 Revision history

Table 52. Revision history

| Document ID | Release date | Description |
|-------------|---------------|-----------------|
| TJA1445 v.1 | ## Month YYYY | Initial version |

Legal information

Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

- [1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <https://www.nxp.com>.

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <https://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

High-speed CAN transceiver with partial networking

Suitability for use in automotive applications — This NXP product has been qualified for use in automotive applications. If this product is used by customer in the development of, or for incorporation into, products or services (a) used in safety critical applications or (b) in which failure could lead to death, personal injury, or severe physical or environmental damage (such products and services hereinafter referred to as “Critical Applications”), then customer makes the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, safety, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. As such, customer assumes all risk related to use of any products in Critical Applications and NXP and its suppliers shall not be liable for any such use by customer. Accordingly, customer will indemnify and hold NXP harmless from any claims, liabilities, damages and associated costs and expenses (including attorneys’ fees) that NXP may incur related to customer’s incorporation of any product in a Critical Application.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer’s applications and products. Customer’s responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer’s applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Contents

| | | | | | |
|----------|---|----------|-----------|---|-----------|
| 1 | General description | 1 | 7 | Limiting values | 41 |
| 2 | Features and benefits | 1 | 8 | Thermal characteristics | 43 |
| 2.1 | General | 1 | 9 | Static characteristics | 43 |
| 2.2 | Predictable and fail-safe behavior | 2 | 10 | Dynamic characteristics | 49 |
| 2.3 | Low-power management | 2 | 11 | Application information | 55 |
| 2.4 | Diagnosis and Protection | 2 | 11.1 | Application diagram | 55 |
| 3 | Ordering information | 2 | 11.2 | Application hints | 56 |
| 4 | Block diagram | 3 | 12 | Test information | 57 |
| 5 | Pinning information | 5 | 12.1 | Quality information | 57 |
| 5.1 | Pinning | 5 | 13 | Package outline | 58 |
| 5.2 | Pin description | 5 | 14 | Handling information | 61 |
| 6 | Functional description | 7 | 15 | Soldering of SMD packages | 61 |
| 6.1 | Supply | 7 | 15.1 | Introduction to soldering | |
| 6.2 | System operating modes | 7 | 15.2 | Wave and reflow soldering | |
| 6.2.1 | Pin and functional block states per operating mode | 10 | 15.3 | Wave soldering | |
| 6.2.2 | Local wake-up via the WAKE pin | 10 | 15.4 | Reflow soldering | |
| 6.3 | CAN operating modes | 11 | 16 | Appendix: ISO 11898-2:2016 parameter cross-reference lists | 64 |
| 6.3.1 | Functional block state per CAN operating mode | 12 | 17 | Revision history | 65 |
| 6.3.2 | CAN wake-up | 13 | | Legal information | 66 |
| 6.3.2.1 | CAN wake-up pattern (WUP) | 13 | | | |
| 6.3.2.2 | CAN wake-up frame (WUF) | 15 | | | |
| 6.4 | Interrupt processing | 18 | | | |
| 6.5 | Device ID | 18 | | | |
| 6.6 | Lock control | 18 | | | |
| 6.7 | General-purpose memory | 18 | | | |
| 6.8 | GPIO pins - TJA1445B only | 18 | | | |
| 6.9 | Failure handling | 19 | | | |
| 6.9.1 | TXD dominant timeout | 19 | | | |
| 6.9.2 | CAN transmitter enable/disable(TXEN_N) - TJA1445B only | 20 | | | |
| 6.9.3 | Bus dominant timeout | 20 | | | |
| 6.9.4 | VBAT undervoltage | 20 | | | |
| 6.9.5 | VIO undervoltage | 20 | | | |
| 6.9.6 | VCC undervoltage | 20 | | | |
| 6.9.7 | Overtemperature | 20 | | | |
| 6.9.8 | MCU reaction timeout | 20 | | | |
| 6.10 | SPI interface | 21 | | | |
| 6.10.1 | SPI error handling | 22 | | | |
| 6.10.2 | SPI system reset | 22 | | | |
| 6.10.3 | SPI register map | 23 | | | |
| 6.10.4 | System control and status registers | 24 | | | |
| 6.10.5 | CAN configuration and status registers | 26 | | | |
| 6.10.6 | GPIO configuration and status registers: TJA1445B only | 27 | | | |
| 6.10.7 | Partial networking registers | 32 | | | |
| 6.10.8 | System reset register | 35 | | | |
| 6.10.9 | Wake-up pulse configuration register | 35 | | | |
| 6.10.10 | Interrupt registers | 35 | | | |
| 6.10.11 | Lock control register | 39 | | | |
| 6.10.12 | General-purpose memory registers | 39 | | | |
| 6.10.13 | Device identification register | 40 | | | |

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.